Oxide-based Complementary Inverters with High Gain and NanoWatt Power Consumption

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Abstract—Oxide semiconductors are ideal candidates for flexible and transparent electronics. Here, we report complementary inverters based on p-type tin monoxide and n-type indium-gallium-zinc-oxide thin-film transistors. The inverters have a gain of 63 at a supply voltage, $V_D$, of 1.5 V with a maximum static power consumption of 15.6 nW, and a gain of 226 at a $V_D$ of 3.0 V with a maximum power consumption of 241.2 nW. A five-stage ring oscillator (RO) based on the complementary inverters are able to operate at 1.04 kHz, with full amplitude oscillations at a $V_D$ of 1.5 V. All the inverters and RO are fabricated on silicon wafers but at a maximum processing temperature of 225 °C, so that the results are relevant to possible flexible applications. The extremely low power consumption of nanowatt, high gain, kHz operation, and possible flexibility of the fabricated complementary components are well suited to meet the requirements of wearable electronics, internet of things technology, etc.

Index Terms—Complementary inverter, indium gallium zinc oxide (InGaZnO or IGZO), tin monoxide (SnO), low-power, high gain, ring oscillator (RO), thin-film transistor (TFT).

I. INTRODUCTION

Oxide semiconductors have been drawing much attention for their high carrier mobility (~1-100 cm2V−1s−1), visible light transparency, low and even room temperature processability, and are therefore ideal candidates for flexible and transparent electronics. [1-4] Complementary inverters based on oxide semiconductor thin film transistors (TFTs) are basic building blocks of digital circuits that are essential in the emerging applications such as wearable electronics and internet of things (IoT) technology.

Recently, inverters based on unipolar n-type oxide like indium gallium zinc oxide (InGaZnO or IGZO) [5, 6], indium gallium oxide [7], and zinc oxide [8, 9], and ambipolar tin monoxide [10, 11] have been demonstrated. However, these inverters commonly have problems of large size, non-full amplitude output voltage swings, low noise margin level, and high power consumptions. Complementary inverter composed of a p-type and an n-type TFTs can well solve such problems. However, there is limited development of high performance p-type oxides [12]. P-type carbon nanotubes (CNTs) [13, 14], organic semiconductors [15, 16], poly-silicon [17, 18], and metal compound [19, 20], are developed to construct complementary inverters with n-type oxides. However, the process compatibility, thermal stability, p-type purity, flexibility, and performances such as supply voltage, gain, and noise margin level are commonly unsatisfactory. Among the reported limited p-type oxides, SnO has been regarded as the most promising due to its high field-effect mobility [21], high stability in ambient air [22, 23], and high on/off current ratio for TFTs based on them [22, 24, 25]. Thereby, complementary inverters based on p-type SnO and n-type oxides, e.g. IGZO, are highly desirable for the next generation of flexible/transparent circuits with low supply voltages high performance [26-28].

To date, the supply voltage of the reported oxides-based inverters still need to be further reduced to meet the requirements of battery-powered or wireless radio-frequency (RF) powered wearable electronics, and IoT technology. Most reported complementary inverters have power consumption in μW level [13-15, 18-20, 26-29]. Only very limited inverters have power consumptions in nW level, however, the low voltage-gains (of ≤20) highly limit their applications [16, 30].

In this work, we have developed complementary inverters based on p-type SnO and n-type IGZO with rather low power consumption of 15.6–241.2 nW, and high gains of 63–226 at low supply voltages of 1.5–3.0 V. In addition, these inverters show high noise margins and high logic-swing output. A ring oscillator (RO) based on the complementary inverters was also fabricated to illustrate its dynamic characteristics in different supply voltages of 1.5–4.5V.

II. EXPERIMENTAL

Figure 1(a) shows the schematic diagram of the fabricated complementary inverters. Si wafers with 300-nm-thick thermally grown SiO₂ were used as the substrates. First, 5-nm-thick Ti for adhesion and 30-nm-thick Au as the gate electrode were deposited by e-beam evaporation and patterned by photolithography. 7.5-nm-thick Al₂O₃ gate dielectric was...
then deposited by atomic layer deposition at a substrate temperature of 100 °C and patterned by photolithography and reactive ion etching. 20-nm-thick p-type SnO was deposited by radio-frequency (RF) magnetron sputtering with Sn target at room temperature (RT). The RF power, working pressure, and oxygen partial pressure (O2/(O2 + Ar)) are 50 W, 5.7 mTorr, and 3.1%, respectively. The sample was then post-annealed at 225 °C for 2h in ambient air. Then, 16-nm-thick IGZO was RF-sputtered with a power of 90 W, a deposition pressure of 3.6 mTorr, in Ar atmosphere at RT. 30-nm-thick Ti was deposited by e-beam evaporation and patterned by photolithography as the source/drain contacts. The width to length ratios of SnO and IGZO channels are 60 µm/20 µm and 20 µm/20 µm, respectively. The sample was then annealed at 150 °C for 1h in ambient air. The current-voltage (I-V) characteristics of the individual TFTs and complementary inverters were characterized at RT in dark by Agilent B2902A source/measure unit. The output waveform of the five-stage RO was measured by Keysight MSO6004A mixed signal oscilloscope.

![Image](image_url)

**Fig. 1.** Schematic view of a complementary inverter based on SnO and IGZO TFTs on a Si/SiO2 substrate (a), transfer (b) (d) and output (c)(e) characteristics of the p-type SnO and the n-type IGZO TFT TFF, respectively.

## III. RESULTS AND DISCUSSION

Figure 1(b) and (d) shows the transfer characteristics of the p-type SnO and n-type IGZO TFTs at the drain voltage of -0.1 and 0.1V, respectively. The SnO and IGZO TFTs exhibit linear-mobility of 0.60 and 12.08 cm²V⁻¹s⁻¹, a sub-threshold swing (SS) of 0.75 and 0.24 V/decade, a threshold voltage (VTH) of -1.61 and 1.87 V, and an on/off current ratio of 1.50x10⁵ and 2.15x10⁶, respectively. The output curves shown in Fig. 1(c) and (e) indicate clear current saturations and ohmic contacts between the source/drain electrodes and the active layers.

Figure 2(a) shows the schematic diagram of the complementary inverter (inset) are the static voltage transfer characteristics (VTCs), indicating almost ideal rail-to-rail output voltage behavior. The threshold voltage of the inverter, where VOUT = VIN, is found to be 0.80, 1.17, 1.30, and 1.47 V at different power supply voltages, VDD, of 1.5, 2.0, 2.5, and 3.0 V, respectively, and all are very close to the ideal value, half value of the VDD. The ultrathin 7.5 nm high-k dielectric Al2O3 layer contributes to the low supply voltages of 1.5~3.0 V, which are extremely desirable for battery-powered or wireless RF powered circuits.

The values of noise margin high NMH and noise margin low NMl, defined as NMH = VOH - VIN and NMl = VIL - VDL, respectively, are summarized in Table I, where VIL and VIN are the input voltage values with the slopes of VTCs equal to -1, VOH is the output-high voltage and VDL is the output-low voltage. Both NMH and NMl are close to the ideal value of VDD/2, indicating excellent noise performance.

Figure 2(b) shows that the inverter has very high output voltage gain, |dVOUT/dVIN|, of 63~226 when operated at VDD of 1.5~3.0 V, as also shown in Table I. Figure 3(a) summarizes the output voltage gains of the reported complementary inverters based on general generation semiconductors including CNTs, 2-dimensional materials, oxides, and metal compounds. Comparing to the reported inverters with gains below 160 [15], the inverter in this work reach the highest gain of 226 at VDD of 3.0 V. The high gain is mainly attributed to the low SS originated from the high channel interface quality and low trap state density in the channels. The high gain and large noise margin of inverters ensure high reliability for the logic gates and complex circuits based on them.

![Image](image_url)

**Fig. 2.** Static voltage transfer characteristics (a) and voltage gains (b) of inverters with aspect ratios R = (W/L)p/(W/L)n and N = 3 at VDD of 1.5, 2.0, 2.5, and 3.0 V.

Figure 3(b) displays the drain current-voltage (IDD-VDD) output curves of the inverter. Pmin and Pmax, which are the minimum static power consumption before switching and the maximum static consumption occurring at the switching point, respectively, are used to fully evaluate the static power consumption, as shown in Table I. Pmin can even reach to pW (2 pW for VDD of 1.5 V) due to extremely low off current of TFTs based on IGZO and SnO with wide bandgaps. Pmax is found to be as low as 15.6~241.2 nW at VDD of 1.5~3.0 V, indicating rather low power consumption during switching.

Figure 3(c) summarizes the VDD of the above mentioned reported inverters [13-20,26-39], commonly in range of 2~100
Our inverter has realized the lowest $V_{DD}$ of 1.5 V, with yet high performance. Such low $V_{DD}$ lead to significantly low power consumption.

In computer science, energy efficiency ratio “performance per watt” is commonly used to evaluate the computation rate of a computer architecture or hardware per every watt consumed. In this work, we introduce the voltage-gain per nanowatt consumed, $|\text{Gain}|/P_{\text{max}}$, to evaluate the energy efficiency of the inverter during switching. Fig. 3(d) summarized the $|\text{Gain}|/P_{\text{max}}$ of the above mentioned reported complementary inverters, and it’s clear that our inverter achieves the most effective performance per watt of 4.0.

**Fig. 3.** Summary of $V_{DD}$ (a), static voltage gains (c), and performance per watt (d) of the reported complementary inverters based on carbon nanotubes or 2-dimensional materials (marked as up triangle in black), n-type oxides and p-type non-oxide semiconductors (marked as circles in blue), n-type oxides and p-type oxides (marked as down triangle in red), and our inverter (marked as star in red). (b) Drain current-voltage ($I_{DD}-V_{DD}$) output curves of our inverter at different $V_{DD}$ of 1.5–3.0 V.

**Fig. 4.** (a) Layout of the five-stage complementary ring oscillator (RO) with an output buffer. Input (b) and output (c) characteristics of the composed inverters. (d) Output voltage of the RO as a function of time at different $V_{DD}$. (e) Oscillation frequency and propagation delay as a function of $V_{DD}$ for the RO.

Figure 4(a) shows the layout of the 5-stage RO with an output buffer. The input pulse, $V_{IN}$, and the corresponding output, $V_{OUT}$, at an operating frequency of 1000 Hz are shown in Fig. 4(b) and (c), respectively. The oscillation frequency, $f$, of the ring oscillator increases from 1.04 to 8.16 KHz with $V_{DD}$ increasing from 1.5 to 4.5 V, as shown in Fig. 4(d) and (e). The stage delay of the RO, calculated as $1/10f$, is found to be 12–66 μs with $V_{DD}$ of 4.5–1.5 V and the whole circuit power current of 24.63–0.74 μA.

**IV. CONCLUSION**

In summary, complementary inverters composed of p-type SnO and n-type IGZO TFTs with rather low supply voltages of 1.5–3.0 V, high gains up to 226, and high noise margin, have been fabricated via low-temperature (maximum 225 °C) process. These inverters with high electrical performance achieve rather low maximum static power consumptions of 15.6–241.2 nW with supply voltages of 1.5–3.0 V. The results would inspire reliable circuit designs and fabrications with low voltage, low power consumption, and flexibility, such as IoT technology and wearable/portable electronics.


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