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Ultrafast Nanoscale Phase-Change Memory Enabled By Single-Pulse Conditioning

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Abstract

We describe how the crystallization kinetics of a suite of phase-change systems can be controlled by using a single-shot treatment via "initial crystallization" effects. Ultra-rapid and highly-stable phase-change structures (with excellent characteristics), viz. conventional and sub-10 nm-size cells (400 ps switching and 368 K for ten-year-data retention), stackable cells (900 ps switching and $10^6$ cycles for similar-'switching-on' voltages) and multi-level configurations (800 ps switching and resistance-drift power-law coefficients < 0.11) have been demonstrated. Material measurements and thermal calculations also reveal the origin of the pre-treatment-assisted increase in crystallization rates, and the thermal diffusion in chalcogenide structures, respectively.
Phase-change memory (PCM) is an excellent candidate for achieving a 'universal' memory structure.\textsuperscript{1,2} PCMs are based on the reversible transition between the amorphous and crystalline states of a chalcogenide material—showing a marked contrast in physical characteristics, e.g. optical reflectance and electrical conductivity, between the phases—of which the $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST–225) system is perhaps the best known.\textsuperscript{3-5} Crystalline GST–225 has also shown interesting thermoelectric properties.\textsuperscript{6} The amorphous-to-crystalline transition is often referred to as “set”, and the crystalline-to-amorphous transition is termed “reset”. However, the rate of crystal nucleation and growth is insufficiently fast compared to that of melting and quenching to the amorphous state, and this limits the overall switching time. Best-performing phase-change structures with archetypal configurations, viz. two-state (0, 1), have exhibited structural ordering using voltage pulses of durations on the order of 1-10 ns.\textsuperscript{7} It is questionable if these times are sufficient for 'universal' memory applications, cf. traditional RAM switching times are around 1 ns.\textsuperscript{8} A difficulty arises from the trade-off between increasing the rate of crystallization and, at the same time, extending the stability of the amorphous phase for long-term data retention.\textsuperscript{9} This has prevented widespread PCM commercialization.

Recently, an incubation-based approach has been used to control crystal nucleation and growth kinetics to furnish crystallization times below 1 ns using conventional GST.\textsuperscript{10} However, such incubation-based systems capable of 500-picosecond crystallization pulses, using a constant low voltage (to produce thermal prestructural ordering) and with multiple low-voltage usage, need to be improved. This is important to
meet the ever-rising demand for faster consumer electronics. This thermal-incubation process is very different from the model of Karpov et al.,\textsuperscript{11} which assumes a direct electric-field-induced modification of the crystal-nucleation barriers in GST. Rao et al. recently pointed out that a not so conventional Sc-doped Sb\textsubscript{2}Te\textsubscript{3} phase-change material without pre-programming has a rapid switching time of 700 picoseconds.\textsuperscript{12}

Melting (and quenching) in the central region of a memory cell can occur, followed by crystallization spatially separated from the centre (Figure 1a). The melting rate is faster at higher temperatures, while rapid crystal nucleation and growth occurs at lower temperatures.\textsuperscript{13} This can be produced by using a voltage pulse of high amplitude and moderate duration (hereafter referred to as a 'shot'.) (Figure 1b) The “melting-and-crystallization” state can show a similar resistivity to that of the bare “reset” state due to the formation of minute crystals spatially separated from the centre. The overall rates of crystal nucleation and growth are essentially increased because of the high surface-to-volume ratio of such minute structures. These crystallites can readily be preserved after reversible switching; the standard moderate-amplitude voltage pulse for “set” switching and high-amplitude voltage pulse for “reset” switching (Figure 1b) archetypally produces crystallization and melting at central regions, respectively. This will permit a 'single'-usage, incubation-based methodology (Figure 1c). The “melting-and-crystallization” state provides a route to achieve a similar stability of the amorphous structure to that for the bare “reset” state, e.g. at annealing temperatures below melting and crystallization temperatures, since the crystal-growth rate is slower at lower temperatures. The melting-and-crystallization phenomenon has been similarly observed using GST-based thin films
using laser pulses, which are excellent prospects for optical memory applications; however, the formation mechanism is still unknown.\textsuperscript{14} Zhou \textit{et al.} have harnessed annealing to obtain a crystalline matrix, and subsequent melting and quenching to form an amorphous region embedded in crystalline templates using promising thin-film SiSbTe-based devices.\textsuperscript{15} However, due to crystallization designed to occupy an entire thin film, the surface-to-volume ratio is often insufficiently high; this has produced an inadequate increase in the rate of crystal nucleation and growth. In addition, BrightSky \textit{et al.} have developed an interesting atomic-layer deposition (ALD) process which can deposit nano-crystalline GST within the pore of a device and the devices can exhibit high-resistance readings, but the formation mechanism remained unclear.\textsuperscript{16}

Here, we control the crystallization rates with a \textit{single-shot} treatment to produce thermal initial crystallization via Joule heating, which permits faster crystal nucleation and growth upon subsequent “set” pulses. A 400-picosecond crystallization pulse and an extrapolated ten-year data-retention temperature of 368 K were achieved for a GST system with an archetypal and below-10 nm structure. This represents the fastest of the current reported PCMs with conventional and sub-10 nm configurations under full recrystallization conditions, and with the use of the voltage-peak full-width-half-maximum (FWHM) as a measure of the pulse duration.\textsuperscript{17,18} A 900-picosecond crystallization pulse and $10^6$ cycles of similar 'switching-on' voltage pulses were also demonstrated using a configuration with a stacked structure. Namely, this is the first demonstration of sub-1 ns switching of a PCM with stacked configurations under full recrystallization conditions, with the use of the voltage-peak FWHM as a measure of the
pulse duration.\textsuperscript{19,20} A system with a multi-level structure also exhibited an 800-picosecond structural-ordering time and resistance-drift power-law coefficients below 0.11. This is about an order of magnitude faster than the fastest switching times of any of the existing PCMs with multi-state configurations under full recrystallization conditions and with the use of the voltage-peak FWHM as a measure of the pulse duration.\textsuperscript{21,22} Material characterization and thermal modelling also elucidate the origin of the pre-pulsing-assisted increase in crystallization rate, and the thermal diffusion in PCM structures, respectively.

We have probed the electrical signatures for a suite of phase-change systems, viz. prototypical and sub-10-nanometre, multi-level and stacked configurations, mainly with GST–225 ‘via’ pore-like structures, using our custom-built electrical testing system\textsuperscript{10} (see Experimental and Modelling Methods in Supporting Information). The archetypal configuration, for instance, comprised silicon-dioxide (SiO\textsubscript{2})-on-Si as the starting structure, on which a 200 nm-thick TiW bottom electrode was formed, followed by the patterning and etching of a 20 nm-thick SiO\textsubscript{2} insulating layer to form pores, which were filled with a 20 nm-thick GST–225 active layer. Finally, a 200 nm-thick TiW top electrode was deposited to complete the structure (Figure 1e). Devices were initially in the high-resistivity state. Some studies were of the 'set-and-cook' type, in which we chose to pre-treat the structures once by using a \(~5.0\text{ V–60 ns} \) voltage pulse. For example, this is about two times shorter in time than the shortest times used for previous studies under negligible crystallization conditions and with the use of the FWHM as a measure of the pulse duration.\textsuperscript{10} This is important to permit energy-efficient memory devices (see
Detailed Electrical and Calculation Analysis in Supporting Information). This was followed by subsequent crystallization from the high- to low-resistance levels, viz. around 300 kΩ and 10 kΩ, respectively (Figure 1c). The duration of the shortest pulse able to crystallize the systems was measured (Figure 1d). Configurations without pre-pulsing were characterized for comparison. We have also examined the effect of temperature on the stability of the system in the high-resistivity phase.

A key finding of the present work is that, whereas conventional systems without pre-pulsing did not show crystal nucleation and growth for voltage pulses with durations less than the DRAM limit of 1 ns, pre-treated structures exhibited crystallization when subject to a sub-nanosecond voltage pulse, viz. around 1.6 ns and 800 ps at ~1.0 V with 5 nm pore configurations for non-pretreated and pretreated systems, respectively (Figure 2a). For example, this is about two times faster for an increase in pre-treatment, and the smallest of current reported PCMs with pore-like structures under full recrystallization conditions. These findings were observed while the data retention for the amorphous phase was not affected, viz. 10 years extrapolated data retention at ~368 K and 372 K for the systems with and without pre-pulses, respectively (Figure 2b). The pre-treated structures also showed reversible and stable switching between the amorphous and crystalline phases with voltage-pulse durations below 1 ns for 10,000 cycles using a 5 nm pore configuration, as well as faster crystallization, e.g. ~400 ps, with an increase in pre-treatment-pulse length (Figures 2c,d). For instance, this is about 20% faster than the fastest times achieved by previous record studies under full recrystallization conditions and with the use of the FWHM as a measure of the pulse duration. The pretreated
system can also show excellent characteristics in terms of time-dependent resistance drift for the amorphous phase, pore-size dependent crystallization time, endurance of the glassy state, crystalline-to-amorphous transition time and crystallization voltage (Figures 2e,f, see Figures S2b,c and Additional Electrical and Modelling Data in Supporting Information). Furthermore, the pretreated system with stacked configurations can exhibit superior properties in terms of crystallization time and stability of the pre-treated system in the low-resistance state, e.g. 900 ps switching and $10^6$ cycles for similar “switching-on” voltages, and the pretreated system with multilevel configurations can show outstanding signatures in terms of crystallization time and time-dependent drift of the resistance levels, e.g. 800 ps switching and resistance-drift power-law coefficients $< 0.11$ (Figures 2g,h, see Figures S2a,4c and Additional Electrical and Modelling Data in Supporting Information). Such fast crystallization facilitated by pre-treatment is indicative of the ease of harnessing the pre-pulsing protocol for PCMs with different systems.

The observation of fast crystal nucleation and growth, facilitated by pre-treatment, therefore gives a clue as to the possible morphology of the system in the pre-pulsed state, namely that it is comprised of crystalline surfaces or structures surrounding an amorphous matrix of GST–225. The significance of ordered configurations for the structures in the pre-pulsed phase has also been noted from electric-field waveform studies, but the component of the pre-treated state, and its structure, has not hitherto been investigated. It is important to note that, by transmission electron-microscopy (TEM) inspection, the pre-treated configuration can show minute ordered structures
(albeit in low concentration) around the glassy region, for instance, near the insulating or electrode layers (Figure 3a). The ordered structures can act as a template for crystal growth, i.e. with negligible nucleation, resulting in a fast crystallization rate,\(^7\) although this direction will be investigated in the future. The pre-pulsed configurations can also show similar crystalline structures after reversible switching (see Figure 3b). It is notable that the non-prepulsed configuration does not show any ordered structures throughout the entire cell (Figure 3c). The ordered structures can be preserved after many reset and set cycles, which is demonstrated from the TEM observations. This is why the effect of the initial pre-pulse can persist during such cycles. These ordered structures do not perniciously affect the thermal-stability properties, as shown in Figure 2b. We speculate that the thermal distribution can be that, during reset, the ordered structures do not completely disappear. This can be very different from the centre of the cell, which is exposed to very high temperatures during the reset, eventually removing the memory of pre-heating, although this will be investigated in future work. This means that amelioration of the crystallization time can be related to the local area near the edge of a cell. Furthermore, theoretical modelling reproduces the high temperatures required for crystal formation near the boundaries of the GST–225 layer at different ends or corners of the GST models, viz. top, right, top right, for both high excitation voltages and moderate durations, e.g. \(~600\) K–700 K (see Figure 1a and Supporting Information Figure S5). The pre-treated systems can also show a low degree of crystallinity, and it is notable that, although we do not observe a pre-pulsed duration shorter than the RAM limit of 1 nanosecond, the pre-pulsing duration is reduced with an increase in pre-pulsed voltage, although experiments to use pre-treatment pulses below a nanosecond will be
investigated in future studies (Figure 1b, see Other Electrical Data in Supporting Information).

It is likely that the voltage and pulse length can influence the type and volume of ordered structures, which can subsequently affect the crystallization time. Experimentally, it can be generally difficult to directly observe the effect of voltage and pulse length on the type and volume of ordered structures, and the effects of type and volume of ordered structures on the subsequent crystallization time. However, our pre-treatment pulse-length experiment is likely to provide some insight. It can be noted that the cell shows a pre-treatment pulse-length dependent crystallization time (Figure 2d). On the one hand, when the pre-treatment pulse is shorter than or equal to around 40 ns, the cell can show a crystallization time that is not so different from those of a cell without pre-treatment. It can be that the small or no influence is related to the possibility that the volume of the ordered structure is negligible or absent. On the other hand, when the pre-treatment pulse is longer than around 40 ns, the cell can show a decreased crystallization time with an increase in pre-treatment-pulse length. This finding indicates that a pre-treatment pulse longer than ~40 ns might be long enough to produce a sufficient volume of ordered structures, so that the crystallization time can be effectively reduced, although future work should be carried out to investigate this effect, including the dependence of the crystallization time or volume of ordered structures on the pre-treatment voltage value, and the influence of the type of ordered structures on the crystallization time, whereby these trends can be similar.
In our switching experiments, the sub-10 nm-sized cell (5 nm-wide pore) without pre-treatment can show a crystallization time of around 1.6 ns (Figure 2a), in contrast to the same-sized cell with pre-treatment which shows a crystallization time of ~400 ps (Figure 2d), i.e. approximately four times shorter compared to the non-pretreated cell. It can be that the crystallization time is always noticeably reduced for the pre-treated cell compared to the non-pretreated cell with the same cell size (Figure 2f, inset). Therefore, even for a very small-sized device, we expect that further improvement can be achieved with pre-treatment in addition to the improvement by scaling alone; so that the best performance can be realized by downscaling with pre-treatment, but without significant degradation of the thermal stability (Figure 2b), which is another requirement for high-density memory.

Thus, the results suggest that rapid, stable, and nanometer-scale switching operations could be produced using conventional, stacked and multi-level systems with a single-shot pre-treatment. By using structures with a higher proclivity for nucleation and growth and, at the same time, showing robustness to spontaneous crystallization, a systematic increase in the rate of switching can be achieved while maintaining a high stability of the amorphous state.

Our work demonstrates fast-switching speed but highly-stable phase-change structures for conventional and sub-10 nm size (viz. 400 ps switching, 368 K for ten-year data retention), stackable cells (e.g. 900 ps switching, $10^6$ cycles for similar 'switching-on' voltages) and multi-level configurations (i.e. 800 ps switching, resistance-drift power-
law coefficients < 0.11) for a single-shot pulse pre-treatment. This pre-treatment method, well suited to the study of the creation of fully ordered minute structures, should be a complementary, and cost-effective, alternative technique to established electrically-based methods, involving field aspects of crystallization, for the rapid optimization of configurations suitable for phase-change memories.

**Associated Content**

**Supporting Information**

The Supporting Information is available free of charge on the ACS Publication Website at… Details of Experimental and Modelling Methods, Additional Electrical and Modelling Data, Detailed Electrical and Calculation Analysis, Other Electrical Data, and Data of Electrical Characterization and Thermal Modelling.

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**Notes**

The authors declare no competing financial interest.

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References


Figure Captions

Figure 1. Single-pulse pre-crystallization effects on the crystal nucleation and growth of phase-change systems. a) Finite-element-method simulations of the temperature distribution in the structure with low (left panel) and high (centre panel) excitation voltages. The pulse duration was kept constant, and the systems were excited by low (around 3.0 V) and high (~5.0 V) pulse voltages, respectively. Right panel: temperature profile of the GST–225 layer with high (red line) and low (blue line) excitation voltages, showing a lower rate of temperature reduction away from the GST–225 centre with an increase in the excitation voltage. b) System resistance (colour scale) as a function of pulse voltage and pulse duration for the structure with an initially high-resistance level. The structure of the system was kept constant (prototypical type), and the sizes of the pores of the configuration were maintained to be the same at around 50 nm. c) Illustration of current work for a voltage pulse with a high amplitude and moderate pulse length for single-pulse conditioning, with a short main pulse used to crystallize the configuration. The single conditioning pulse is harnessed for initiating crystal formation around the glassy material, followed by the main pulse, viz. in (d), to induce structural ordering of the system. e) The PCM structure, along with a photograph of the device and an atomic-force-microscope image of the pore, used for crystallizing the system (see Supporting Information Figure S1).

Figure 2: Pre-treatment dependence of the crystallization rate and amorphous-phase stability of chalcogenide structures. a) Electrical voltage as a function of pulse
duration needed for crystallizing phase-change memory cells with a conventional configuration (Figure 1e) with (purple line) and without (yellow line) pre-pulsing. b) An Arrhenius extrapolation for 10-year data retention (of the amorphous state) of the prototypical structure with (green line) and without (orange line) pre-pulsing. Supporting Information Figure S2f also shows the Arrhenius extrapolation for 10-year data retention obtained from experiments carried out on a different structure, and this structure also showed similar signatures. c) Plot of the resistance level as a function of the cycle number of a phase-change structure with pre-treatment with constant voltage pulses, e.g. high- to low-resistance levels, around 1.0 V, 800 ps; low- to high-resistance levels, about 5.0 V, 500 ps. d) Plot of crystallization-pulse duration as a function of pre-treatment-pulse duration for the pre-treated structure. The crystallization- and pre-treatment-pulse voltages were kept constant at around 1.0 V and 5.0 V, respectively. e) Time evolution of the resistance level of the archetypal system with and without pre-pulsing (blue and pink lines), with a resistance-drift coefficient, v, determined by a fit to a power law. The ambient temperature was kept constant at around 300 K. f) Pore-size dependence of pulse length with pre-treatment for crystallizing the structure under a constant pulse voltage (~1.0 V). The inset shows a table of the pulse length for crystallizing the pre-treated system and the non-pretreated system and with different pore sizes, showing a decreased crystallization time for the pretreated structure compared to the non-pretreated structure for the same pore size. g) Correlation between the voltage amplitude and pulse duration with (blue bars) and without (orange bars) pre-pulsing to crystallize the system with a stacked configuration for constant pore size (about 35 nm). The right panel shows the configuration of the structure. The systems were switched between high- and low-
resistance levels of about 350 kΩ and 190 kΩ, respectively, which are higher than the values for the conventional structure (around 300 kΩ and 10 kΩ), owing to an additional switching layer in the active region of the device. **h)** Resistance (colour scale) as a function of voltage and for varying pulse durations with and without (right and left panels) pre-treatment to crystallize the structure with a multi-level configuration. The systems were switched between the high-, intermediate- and low-resistance levels of about 300 kΩ, 150 kΩ and 10 kΩ, respectively. The coloured boxes show the average of the values obtained from experiments carried out on three different structures. The structures for (a, b, c, d, e, f, h) were initially in the high-resistance level (~300 kΩ), and the sizes of the structures for (a, b, c, d, e, h) were maintained to be the same at around 5 nm. The structure with pre-treatment for (a, b, c, e, f, g, h) was subjected to a voltage pulse (around 5.0 V, 60 ns) in a single-pulse conditioning, while the non-treated system remained untouched. The error bars show the range of values obtained from experiments carried out on three different structures.

**Figure 3.** Pre-treated PCM morphology. **a)** Transmission-electron-microscope (TEM) images of the system with pre-pulsing, showing clusters are formed around the amorphous matrix when pre-treatment is used. **b)** TEM image obtained from experiments carried out on a different structure (after reversible switching). The structure also showed similar morphologies. **c)** TEM image of the system without pre-pulsing. The non-prepulsed system does not show any ordered structures throughout the entire cell, although part of the cell is shown in the figure. For (a-c), the device structure was kept constant (prototypical type), and the pore size of the system was fixed at around 50 nm.
The voltage amplitude and pulse duration for the pre-treatment were kept constant at approximately 5.0 V and 60 ns, respectively. The system was initially in the high-resistance state of about 300 kΩ. The yellow dotted regions indicate the ordered structural regions.
Figures

**Figure 1.**
**Figure 2.**
Figure 3.
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