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Charge-trapping memory based on tri-layer alumina gate stack and InGaZnO channel

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ABSTRACT

Amorphous InGaZnO (IGZO) charge-trapping memory (CTM) devices have been designed and demonstrated entirely with thin-film technologies. All three key layers for blocking, charge-trapping, and tunneling in gate stack are made by Al_2O_3 grown by atomic-layer deposition but with different oxygen sources, i.e., O_3 or deionized H_2O, to achieve different properties. X-ray photoelectron spectroscopy reveals that few defects exist in the H_2O-Al_2O_3 film with only Al-O bonding, while more residual C-related impurities appear in the O_3-Al_2O_3 film leading to a high density of defects, which serve as the charge-trapping states in the gate stack of the CTM devices. The fabricated IGZO CTM can be programmed under a positive voltage bias, and a large memory window of 8.2 V can be obtained with a programming voltage of +20 V. Multi-level storage has been achieved in the fabricated IGZO CTM, and a 1.9 V wide margin between the adjacent two states could be maintained for more than 10 years according to the trend of the data. With light illumination, the memory device can be erased entirely under a negative bias of -5 V. The IGZO CTM devices may have promising potentials for multi-level-storage nonvolatile memory applications based on thin-film technologies.

KEYWORDS: Charge-trapping memory, Al_2O_3, O_3, InGaZnO, Multi-level storage

1. INTRODUCTION

Traditional flash memories are suffering from the miniaturization limit due to high integration density, reliability, and lithography techniques.[1] Since the first three-dimensional (3D) NAND array was proposed in 2007 by Toshiba corporation,[2] alternative methods to improve the storage capacity are pursued by major memory manufacturers, resulting in the first commercial product in Samsung Electronics until 2013.[3] Charge-trapping memory (CTM) based on $SiO_2/Si_3N_4/SiO_2$ (ONO) gate stack structure is the key element of 3D NAND.[2] However, the CTM devices suffer from quick charge loss due to charge detrapping through the thin tunneling layer. Fortunately, the suppression of tunneling current can be realized by using thick high-*k* dielectric films, which are prospective for substituting the traditional ONO gate stack to realize large memory window, low operation voltage, and high program and erase speed.[4] Among the well-known high-*k* materials, Al_2O_3 is a very promising candidate due to the high dielectric constant ($k \sim 9.0$) and the relatively high band gap ($E_g \sim 8$ eV).[5] In our previous work, Al_2O_3 film grown by atomic-layer deposition (ALD) has been demonstrated to be a highly reliable gate insulator.[6] Furthermore, Al_2O_3 has been investigated as tunneling/blocking layers in the CTM devices, due to the superior thermal and chemical stability and the strong adhesion to dissimilar materials.[1, 7] Al_2O_3 was also proposed to be used as the charge-trapping layer in the CTM devices, which showed good retention characteristics, but a small memory window caused by the low trap density.[4] Doping different elements, such as Ta,[8] Ti,[9] and Hf,[10] into Al_2O_3 layer could increase the trap density and the memory window. Shallow traps in these films lead to a poor retention performance. However, large memory window and reliable retention characteristics are crucial for multi-level-storage memory. Researchers have reported the effects of different ALD oxygen sources (H_2O, H_2O_2, and O_3) on Al_2O_3 films during the deposition, and found that H_2O has ideal ligand exchange reactions with trimethylaluminum (TMA), while O_3 leads to a high density of impurities in the film under a low growth temperature.[11, 12] By using different oxygen sources, defect-rich and few-defect dielectric Al_2O_3 layers could be achieved, which can act as charge-trapping and tunneling/blocking layers, respectively.

With increasing the number of 3D NAND gate stack layers, a small cell current with large fluctuation originating from grain and/or interfacial traps in the traditional poly-silicon (poly-Si) channel material is a severe problem.[13-15] It's essential to find new channel materials to meet the 3D memory demand. Amorphous InGaZnO (IGZO) first proposed by Hosono et al. in 2004 has been widely studied due to its excellent characteristics, including high electron mobility, low off current, large-area mass-production compatibility, and low process temperatures.[16] In our previous works, we have also proposed the low power applications of IGZO TFTs based on various high-κ dielectric layers.[6, 17, 18] As a promising channel material, low-temperature-fabricated IGZO was also reported to be used in the CTM devices, which may be applied in flexible and wearable electronics.[9, 19-24] During the manufacturing process of 3D NAND devices, conformal characteristics of films are quite important. Highly conformal films can be achieved by ALD and sputtering technologies, which allow precise thickness control. Recently, high-performance ALD-grown IGZO thin-film transistors (TFTs) have been realized, which means that IGZO can satisfy 3D manufacturing processes.[25]

In this work, the memory characteristics of the CTM devices based on triple-layer ALD-alumina gate stack and IGZO channel layer have been systemically investigated. To achieve excellent non-volatile memory (NVM) properties, low-defect Al_2O_3 films grown with TMA and deionized H_2O (denoted as H_2O-Al_2O_3) were used as blocking and tunneling layers, meanwhile the defect-rich Al_2O_3 film grown by substituting O_3 for deionized H_2O as the oxygen source (denoted as O_3-Al_2O_3) was used as the charge-trapping layer. The defects in O_3-Al_2O_3 film were identified through X-ray photoelectron spectroscopy (XPS) measurements. Al/Al_2O_3/n-Si (MOS) capacitors were also fabricated to determine the trap densities in H_2O-Al_2O_3 and O_3-Al_2O_3 layers. The achieved IGZO CTM devices showed multi-level storage with a good reliability, which have a great promise for the future nonvolatile memory applications.

2. EXPERIMENTAL SECTION

First, bottom gate electrodes with 5 nm Ti and 30 nm Au layers were deposited on a cleaned Si/SiO_2 substrate by electron-beam evaporation. For the CTM devices, 15, 10, and 5 nm Al_2O_3 layers were grown on the gate electrodes by ALD at a low temperature of 150 °C successively, serving as blocking, charge-trapping, and tunneling layers, respectively. Deionized H_2O and TMA were used in the growth of blocking and tunneling layers. During the charge-trapping layer growth, O_3 substituted for deionized H_2O as the oxygen source. During the homogeneous tri-layers Al_2O_3 growth, the dose time of TMA, H_2O and O_3 was 0.03 s, 0.015 s, and 5 s, respectively. There is a 30 s purge process after every dose operation. The precursors were carried by high purity N_2 gas and introduced to the reactor chamber with a chamber pressure of 0.15 Torr. To verify the charge-trapping performance of the CTM devices, the control samples (TFTs) based on 30 nm H_2O-Al_2O_3 film were also prepared. The 24 nm IGZO layer was deposited by radio-frequency (RF) sputtering at room temperature with a 90 W sputtering power under a 3.70 mTorr pressure. Ti source/drain electrodes were then deposited by electron-beam evaporation. The length and width of active channels were both 10 μm. The channel and electrodes were all patterned by photolithography. The trap densities in the Al_2O_3 layer grown under different conditions were explored by fabrication of $Al/Al_2O_3/n$-Si capacitors. These devices were characterized by the capacitance-voltage (*C-V*) and current-voltage (*I-V*) measurements using the Keysight Technologies B1500A semiconductor device analyzer. Two types of Al_2O_3 films were also examined by XPS after Ar^+ ion etching with ThermoFisher ESCALAB 250XI equipment.

3. RESULTS AND DISCUSSION

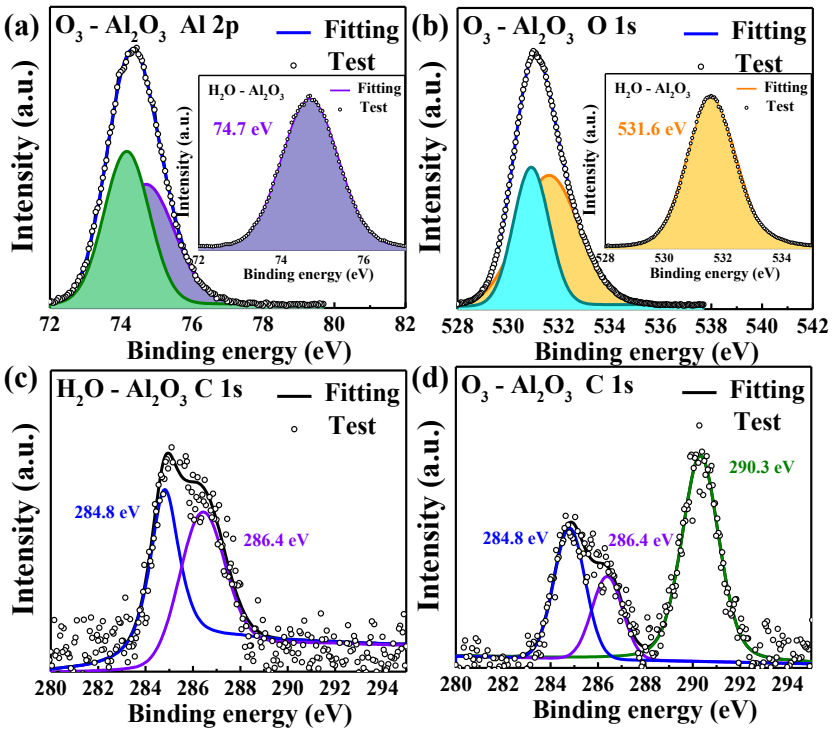

Figure 1. (a) Al 2p, (b) O 1 s core levels for O_3-Al_2O_3 film (main graph) and H_2O-Al_2O_3 (inset). C 1 s core levels for (c) H_2O-Al_2O_3 film and (d) O_3-Al_2O_3, respectively.

The narrow-scan XPS spectra of Al 2p and O 1s of Al_2O_3 films are shown in Figs. 1(a) and 1(b), respectively. All the XPS spectra were calibrated with C 1s peak of 284.8 eV. For H_2O-Al_2O_3 film, core level spectra of Al 2p and O 1s were fitted well as a symmetrical single peak at 74.7 eV and 531.6 eV for Al-O bonds, respectively. Besides the above peaks, additional peaks at 74.2 eV for Al 2p and at 530.9 eV for O 1s have been detected, respectively, in O_3-Al_2O_3 film. During the ALD processes, ideal ligand exchange can be accomplished between H_2O and TMA even at a low growth temperature.[5] However, O_3 eliminates the ligands in TMA molecule by oxidation of the ligands, which needs to overcome a high reaction barrier.[26, 27] During the O_3-Al_2O_3 film growth, the imperfect ligand oxidation state may occur due to the low ALD growth temperature (150 °C). The peaks at 74.2 eV for Al 2p and at 530.9 eV for O 1s may originate from the different oxidation states in the film, such as Al-COOH and Al-OH species.[11, 28] What's more, various residual C-related impurities were also detected in O_3-Al_2O_3 film. Fig. 1(c) shows the C 1 s core level spectra for H_2O-Al_2O_3 film, which was combined with two peaks at 284.8 eV and 286.4 eV corresponding to C-C bonds resulting from the ambient and/or the pump oil vapor pollution in the XPS tool, and

the residual methyl from TMA, respectively. While, there was one more obvious peak at 290.3 eV in O_3-Al_2O_3 film, which could be caused by the C-related oxidation states, such as Al-CO_3 and Al-COOH,[11] as shown in Fig. 1(d). These states at 290.3 eV in O_3-Al_2O_3 film may result from the slow decomposition of O_3 at low ALD growth temperature,[29] which was almost disappeared in the XPS spectra after elevating the growth temperature (such as 250 °C, not shown here). The measured relative atomic percentage of C is about 0.9% and 2.2% for H_2O-Al_2O_3 and O_3-Al_2O_3, respectively, which means there are more C-related impurities existed in O_3-Al_2O_3 leading to more traps in the film.

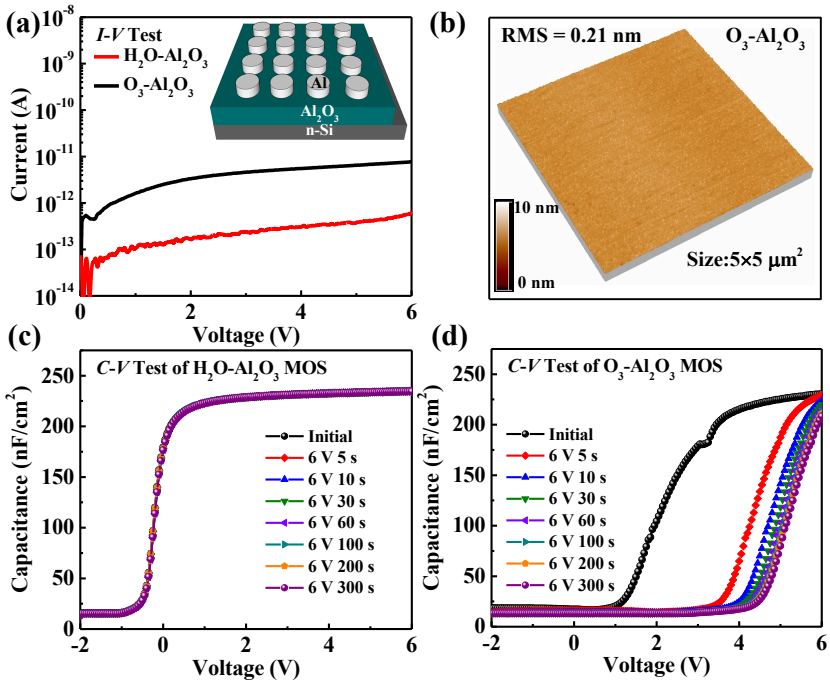

Figure 2. (a) *I-V* measurements (main graph) and schematic diagram (inset) of MOS capacitors based on 30 nm H_2O-Al_2O_3 and O_3-Al_2O_3 dielectrics. (b) AFM image of 30 nm O_3-Al_2O_3 layer grown on n-Si. *C-V* measurements with a constant 6 V bias stress of MOS devices based on 30 nm (c) H_2O-Al_2O_3 and (d) O_3-Al_2O_3 layers.

The dielectric characteristic and trap density of H_2O-Al_2O_3 and O_3-Al_2O_3 films were further investigated by fabricating Al/Al_2O_3/n-Si (MOS) devices. Fig. 2(a) shows the *I-V* measurements and the schematic diagram of the MOS capacitors based on 30 nm Al_2O_3 films. As seen in Fig. 2(a), the leakage current through the O_3-Al_2O_3 film was founded to be more than one order of magnitude larger than that for the H_2O-Al_2O_3 film. As is well known, large surface roughness of film will result in the large leakage current. However, the O_3-Al_2O_3 film showed a smooth surface with the

root-mean-square (RMS) roughness of 0.21 nm, as shown in Fig. 2(b), which was very similar to our previous reported 0.28 nm roughness for H_2O-Al_2O_3 with the same film thickness.[6] Using O_3 as the oxygen source, the chemical reaction between TMA and O_3 may be incomplete, especially at a low temperature, which will lead to much C-related impurities in the Al_2O_3 dielectric layer.[11] Thus, the large leakage current of O_3-Al_2O_3 may be ascribed to the more defects in the film rather than the film surface roughness. These defects could act as charge trapping centers in the film, and *C*-*V* measurements could be used to explore the charge trapping density through the flat band voltage shift (ΔV_{fb}) after a constant voltage stress. The ΔV_{fb} after a 6 V voltage stress from 5 s to 300 s were showed in Figs. 2(c) and 2(d), and the density of trapped oxide charge (N_t) can be obtained from the ΔV_{fb} using the equation of $N_t = (C_{max}\Delta V_{fb})/qA$, where C_{max} is the maximal value of capacitance, and A is the electrode area.[30] After a 300 s constant bias stress, the *C*-*V* curves were slight changed for H_2O-Al_2O_3 device. However, there was a 2.32 V shift of V_{fb} for O_3-Al_2O_3 capacitors. The calculated trap density for O_3-Al_2O_3 device is 3.62×10^{12} cm^{-2}, which is more than two order of magnitude higher than 1.83×10^{10} cm^{-2} for the H_2O-Al_2O_3 film. We also tested the retention characteristics of Al/O_3-Al_2O_3/n-Si MOS devices after a 6 V constant voltage stress for 10 s. The V_{fb} value kept almost unchanged during 10^4 s, as shown in Fig. S1, which means few electrons escaped from the traps. If electrons were trapped by the shallow traps, they would detrap from the shallow traps and the V_{fb} would shift to the initial state. So, this suggests that electrons were trapped in deep level traps. For CTM applications, the high trap density in the charge-trapping layer is benefit for a large memory window, and fewer defects are necessary for tunneling and blocking layers.[4] It means that we can use the Al_2O_3 layer as charge-trapping or blocking layers by manipulating the defects level through changing the oxygen sources of ALD Al_2O_3 films.

Based on above experimental results, IGZO CTM devices with homogeneous Al_2O_3 gate stack have been fabricated, and the device structure is shown in the inset of Fig. 3(d). The densified H_2O-Al_2O_3 layers were used as blocking and tunneling layers, and the defect-rich O_3-Al_2O_3 film was chosen as the charge-trapping layer. To examine the memory properties of IGZO CTM devices,

program processes with different programming voltages (V_P) and programming time (t_P) were firstly investigated. During the program processes, the source and drain electrodes of the IGZO CTM devices were grounded, and a fixed stress voltage was applied on the gate electrode for different time. Fig. 3(a) shows the transfer characteristics of IGZO CTM after programming at 20 V with different t_P from 1 μs to 1 s. A continuously parallel positive shift can be found from the transfer (I_D-V_G) curves without obvious accompanying degradation in subthreshold swing (*SS*). The threshold voltage shift (ΔV_{th}), which is also the memory window, as a function of t_P under different V_P was summarized in Fig. 3(c). The value of ΔV_{th} greatly increased under large programming gate voltage and long programming time, which means that more electrons can get enough energy to tunnel into defect-rich charge-trapping O_3-Al_2O_3 layer. Fig. 3(b) shows the transfer curves of IGZO CTM after different V_P of 1 s. The relationship between ΔV_{th} and programming voltage was summarized in Fig. 3(d). ΔV_{th} is about 8.2 V at a programming voltage of +20 V for 1 s, indicating a good charge-storage capability of the IGZO CTM.

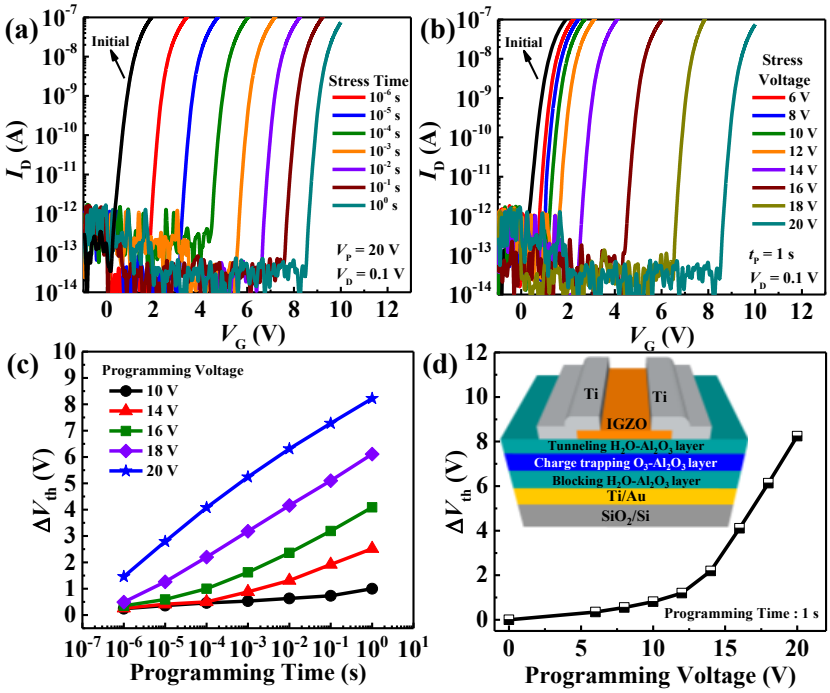

Figure 3. Transfer characteristics of IGZO CTM (a) after operation at 20 V with different t_P, and (b) after operation at 1s with different V_P. The "Initial" curve stands for the devices without program process. ΔV_{th} as a function of the (c) t_P with different V_P and (d) different V_P with 1 s t_P. The inset is the structure image of IGZO CTM devices.

As the control samples, the program processes of IGZO TFTs based on 30 nm H_2O-Al_2O_3 film

were evaluated to further demonstrate the charge-trapping capability of O_3-Al_2O_3. The transfer and output characteristics of the controlled IGZO TFTs are shown in Figs. 4(a) and (b), respectively. The TFTs exhibit a well-defined pinch-off behaviour with a high saturation mobility (μ_{sat} = 10.96 cm^2/Vs), a small subthreshold swing (SS = 112 mV/dec), and a high on/off current ratio (I_{on}/I_{off} = 8.6×10^8). The hysteresis of TFTs was extremely small and the leakage currents were suppressed well, which means that the H_2O-Al_2O_3 played good roles as an excellent gate dielectric layer. Figs. 4(c)-4(e) show the stress time dependence of IGZO TFTs transfer curves after operation at 10, 15, and 20 V stress voltages, respectively. There were almost no changes of transfer curves, when the stress voltages were 10 V and 15 V. Even under a large stress voltage of 20 V, the threshold voltage shift was only ~0.35 V, which can be neglected compared with 8.2 V memory window for O_3-Al_2O_3 CTM devices. Thus, the charge-storage capability of CTM devices was mainly benefited from the defect-rich O_3-Al_2O_3 among the homogeneous gate stacks.

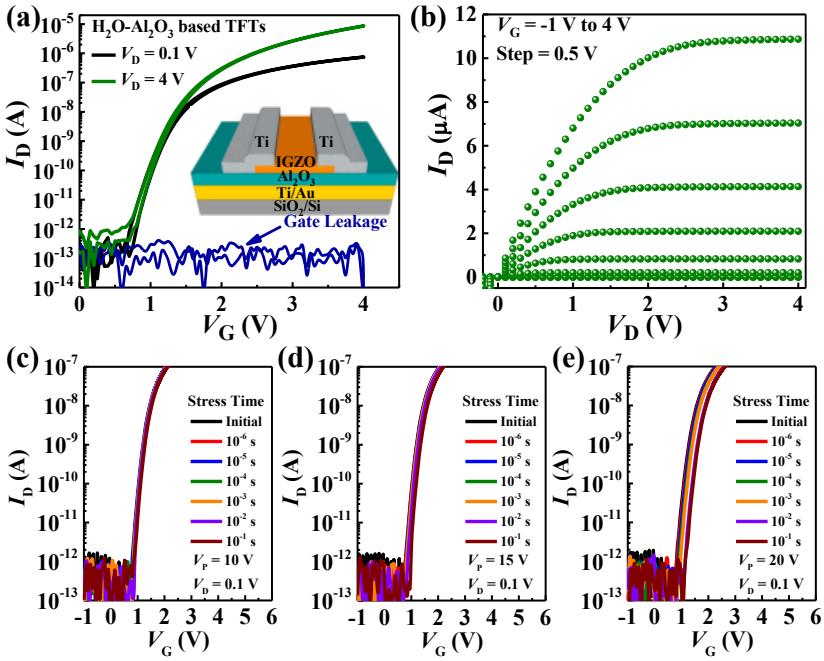

Figure 4. (a) Transfer and (b) output characteristics of the IGZO TFTs. The stress time dependence of the IGZO TFTs after operation at (c) 10 V, (d) 15 V, and (e) 20 V stress voltages, respectively.

The energy band conditions of the Al_2O_3 films were also investigated by XPS measurements. Fig. 5(a) shows the O 1s electron energy loss spectra from two types of Al_2O_3 films. The values of

energy gap were calculated to be 6.99 eV and 6.21 eV for H_2O-Al_2O_3 and O_3-Al_2O_3, respectively. A band gap narrowing was happened in O_3-Al_2O_3 film, as shown in Fig. 5(c). The band edge of the carbon-related defects in the O_3-Al_2O_3 film may shift deep into the forbidden gap, which could form band tails gap and reduce the effective band gap of the film.[31, 32] The valence band offset (ΔE_V = 0.45 eV) of the Al_2O_3 films was calculated from the valence band spectra, as shown in Fig. 5(b). Furthermore, the conduction band offset (ΔE_C = 0.33 eV) can be derived by the equation of $\Delta E_C = E_g(H_2O\text{-}Al_2O_3) - E_g(O_3\text{-}Al_2O_3) - \Delta E_V$. The IGZO bandgap was reported about 3.0~3.3 eV.[19] Thus, we can get the energy band schematic diagrams of IGZO CTM devices in flat band and programming states, as shown in Fig. 5(d) and 5(e). For further improving the performances of CTM devices, such as faster programming speed, larger memory window, and better retention characteristics, the band engineering may be applied to our IGZO CTM devices.[33-35]

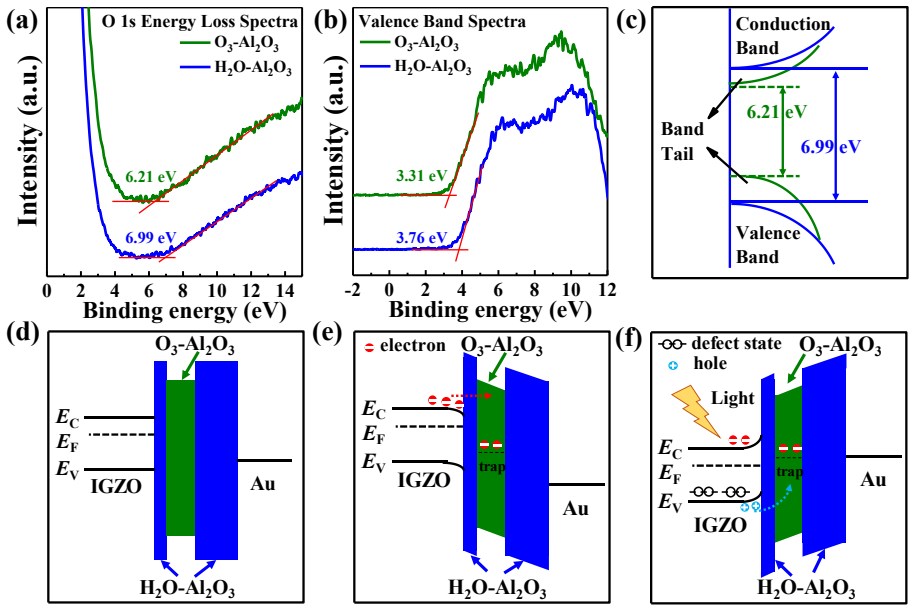

Figure 5. (a) O 1s electron energy loss spectra and (b) valence band spectra of Al_2O_3 films. (c) Carbon-related defects induced band gap narrowing effects in O_3-Al_2O_3 film. Energy-band diagrams of IGZO CTM devices in (d) flat band state, (e) programming, and (f) erasing processes with light illumination.

Erasing characteristics of the IGZO CTM were investigated after a +20 V V_P for 1 s, as shown in Fig. 6(a). The erasing characteristics of the device programmed with different stress voltages are shown in Fig. S2(a). However, the n-type IGZO channel material only supplies electrons due to Fermi level pinning.[36] During the erasing process, even we applied a high negative gate voltage (-

20 V) on the devices, the V_{th} shift is not obvious, only 1.5 V ΔV_{th} with 1 s stress, as shown in the inset of Fig. 6(a). Very few holes can be trapped into the charge-trapping O_3-Al_2O_3 layer under negative gate bias voltages. As such, a LED light source with the wavelength of 450~460 nm and power density of 3 mW/cm^2 was used during the erasing processes. Light erasing processes were also reported in a few other IGZO CTM devices.[19, 37, 38] It was reported that IGZO has some subgap defect states above the valence band maximum (VBM), holes can be generated under exposure to light with a photon energy (~2.3 eV, which is corresponding to ~540 nm).[39, 40] So, as shown in Fig. 5(f), under light illumination, a large amount of electron-hole pairs may be excited in the IGZO channel by enough photons with sufficient energy, and some holes with enough energy could get through the tunneling layer and neutralize the trapped electrons in the O_3-Al_2O_3 layer.[19, 37, 38] Under light illumination, the memory device can be erased entirely under a small negative bias of -5 V for 100 ms. More efforts need to be done to achieve erasing step without light, such as modifying the energy level of the defects in the charge-trapping layer.[34]

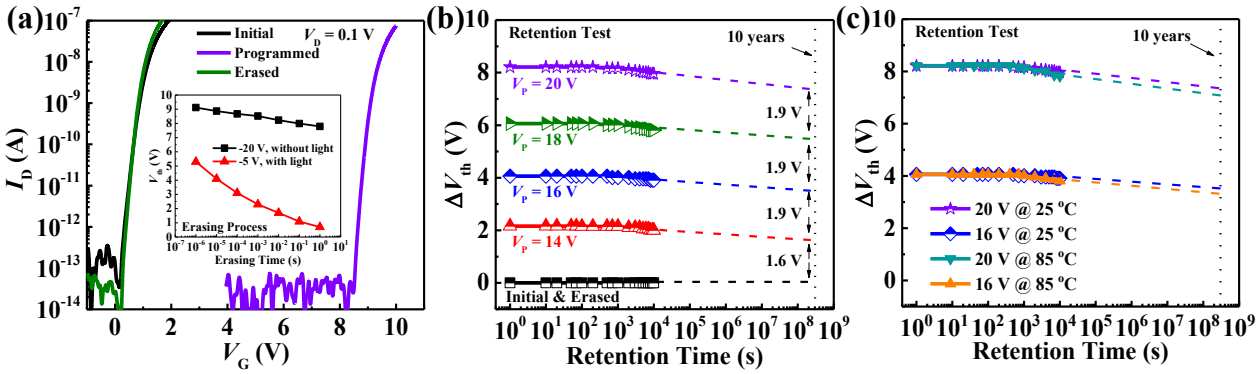

Figure 6. (a) The comparison of erasing process with or without light condition. The multi-level storage retention characteristics of the IGZO CTM at (b) 25 °C and (c) 85 °C.

Fig. 6(b) shows the multi-level storage retention characteristics of the IGZO CTM devices at room temperature (25 °C). During the retention measurements, source, drain, and gate electrodes were all at zero biases after programmed by different stress voltages for 1 s. The threshold voltage kept almost unchanged for CTM devices without programming process and after erased to the initial states. The retention data of the programmed device after being partially erased with light is shown in Fig. S2(b). According to the trend of data showing by the dashed lines in Fig. 6(b), a large

memory window of 7.3 V after 10-year retention is deduced with a 0.9 V retention loss and about 11.0 % charge loss. Multi-level-storage states were also achieved in our IGZO CTM, which were programmed with 14, 16, 18, and 20 V different voltages, respectively. And a 1.9 V wide margin between the adjacent two states could be maintained for 10 years according to the trend of data. The retention characteristics at 85 ºC are shown in Fig. 6(c). Comparing with the threshold voltage at 25 °C, there is only a ~0.3 V decrease after 10 years for the same programming state. The device performance showed a slight decay at a high temperature, which may be caused by the thermally activated charge detrapping.[20] The good retention characteristics of the IGZO CTM devices may be attribute to the deep trapping levels of electrons in the O_3-Al_2O_3 charge-storage layer, which is benefit for realizing multi-level memory applications.

4. CONCLUSIONS

In summary, IGZO charge-trapping memory (CTM) was fabricated with a homogeneous triple-layer alumina dielectric grown by atomic-layer deposition consecutively at 150 ºC temperature. By using different oxygen sources, the obtained Al_2O_3 layers were shown to be capable of acting as the tunneling layer, the charge-trapping layer and the charge-blocking layer. The chemical constituents of the two types of Al_2O_3 films have been analyzed by X-ray photoelectron spectroscopy, and the charge-trapping states in O_3-Al_2O_3 may be caused by the residual C-related oxidation states. A large memory window of 8.2 V was obtained by programming voltage of +20 V. And multi-level storage was achieved in our IGZO CTM after different programming voltages. The IGZO CTM devices may have promising potentials for multi-level-storage nonvolatile memory applications with the advantages of being based on thin-film technologies and having a simple structure for manufacturing.

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