MANCHESTER
1824
The University of Manchester
The University of Manchester Research

Improvement on well design and operation of potential well barrier diodes

DOI:
10.1109/SMICND.2019.8923974

Document Version
Accepted author manuscript

Link to publication record in Manchester Research Explorer

Citation for published version (APA):
Akura, M., Dunn, G., & Missous, M. (2020). Improvement on well design and operation of potential well barrier diodes. In *2019 42nd International Semiconductor Conference, CAS 2019 - Proceedings* (pp. 169-172). Article 8923974 (Proceedings of the International Semiconductor Conference, CAS; Vol. 2019-October). IEEE. https://doi.org/10.1109/SMICND.2019.8923974

Published in:
2019 42nd International Semiconductor Conference, CAS 2019 - Proceedings

Citing this paper
Please note that where the full-text provided on Manchester Research Explorer is the Author Accepted Manuscript or Proof version this may differ from the final Published version. If citing, it is advised that you check and use the publisher's definitive version.

General rights
Copyright and moral rights for the publications made accessible in the Research Explorer are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

Takedown policy
If you believe that this document breaches copyright please refer to the University of Manchester's Takedown Procedures [http://man.ac.uk/04Y6Bo] or contact uml.scholarlycommunications@manchester.ac.uk providing relevant details, so we can investigate your claim.

Download date:20. Sep. 2024

Improvement on Well Design and Operation of Potential Well Barrier Diodes

M. Akura*, G. Dunn* and M. Missous**
*Department of Electronic Engineering, University of Aberdeen, AB25 3UE, UK
E-mail: r01mja16@abdn.ac.uk, g.m.dunn@abdn.ac.uk
**Department of Electronic Engineering, University of Manchester, M13 9PL, UK
Email: m.missous@manchester.ac.uk

Abstract—The flexibility in design of the potential well in PWB diodes has shown promising prospects for zero-bias operation capability and improvements in the overall performance of the diode. We consider the right intrinsic region whilst regrading further the GaAs well. The performance of the diodes was measured and compared in terms of the turn-on voltage and curvature coefficient. We found that the turn on voltage of the diodes improves significantly with increases in the graded regions. At a current density of $\mathbf{0.5 \times 10^{-12}}$ Amperes per meters square, the diodes with graded regions $\mathbf{0.01}$, $\mathbf{0.03}$ and $\mathbf{0.05}$ $\mathbf{mircons}$ have turn-on voltages of $\mathbf{0.85}$, $\mathbf{0.5}$ and $\mathbf{0.38\,Volts}$, while the curvature coefficient estimated at $\mathbf{0.5\,V}$ was respectively obtained to be $\mathbf{6.4}$, $\mathbf{10.3}$ and $\mathbf{20.1\,per\,volt}$.

Keywords—Monte Carlo model; turn-on voltage; barrier height; curvature coefficient; responsivity.

1. Introduction

Just like Planar Doped Barrier diodes (PDB) [1], [2] and other heterostructure barrier devices, Potential Well Barrier diodes (PWB) studied in [3-6] have shown prospects of applications in detector and mixers. The diode has a lot of advantages compared to similar devices for the same purpose. For example, the metal-semiconductor junction of the Schottky barrier diode limits optimum control to the barrier height of the diode [7]. Also, in the planar doped barrier (PDB) diode, the barrier height and depletion region thickness are determined by accurate control of the δ - doping profile. This reduces the degree to which barrier height can be adjusted to achieve zero bias detection [8], [9]. In the PWB diode however, there is flexibility in the potential well design for improving the diode performance without necessarily making changes to the compositional structure of the diode. This technique is achieved by regrading some percentage of the *Al* from the *GaAs* well into $Al_{0.3}Ga_{0.7}As$ over regions of $0.01, 0.03$ and $0.05\ \mu m$. In this paper, we will elucidate how this technique could be used to reduce the barrier height of PWB diodes whilst maintaining a constant reverse bias operation. We will also show the behavior of carriers with respect to electric field, and density of electrons in the potential well.

2. Well Designs and Simulation

Fig. 1.0 (a) illustrates the schematic diagram of a PWB diode while (b) shows some possible designs of well shape; the wall of the well at the right intrinsic region is shifted by 0.01, 0.03 and $0.05\ \mu m$ to the right. The three cases are simulated using Monte Carlo and the drift-diffusion models and results compared for the $I - V$ characteristics, electric field across the diode and density of charge in the potential well. The diode was simulated with left and right intrinsic regions of $700\ nm$ and $150\ nm$ respectively with a *GaAs* well thickness of $30\ nm$.

The MC model has been discussed in previous report on the PWB diode [3], [6] and for the study of Gunn diodes [10] and has been successfully proven to be an effective tool for studying such similar structures especially at high electric fields where consideration to carrier heating is of utmost importance. The scattering mechanism used in the simulation are the inter-valley, acoustic and polar phonon scattering and the effect of non-parabolicity was considered. A constant discretization time step was used; this helps to track time evolution of electron distribution and to determine the points of all sample electrons across the diode. The electron densities at mesh points were calculated and this was

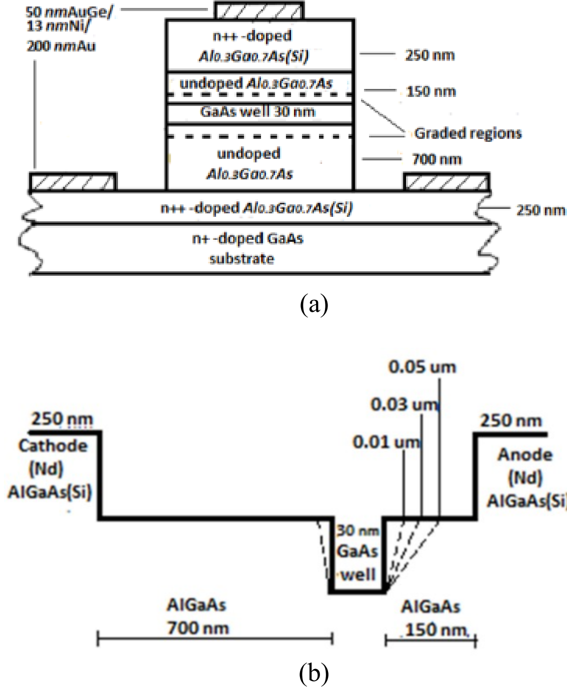

Fig. 1 PWB showing (a) schematic diagram [4] and (b) Equivalent structure and how the potential well can be regraded Schematic. The edge of the well on the right intrinsic regions is moved at distances of 0.01, 0.03 and 0.05 μm to the anode.

followed by computation of the electric field at mesh points using the Poisson equation. A constant lattice temperature of $300\,K$ and band offset of $25\,eV$ was used throughout the simulations.

3. Discussion of Results

A. Current-voltage operation of diode

The $I - V$ characteristics of the diodes is as shown in Fig. 2. This illustrates the behavior of current with respect to the applied voltage in each of the diodes.

There seems to be greater improvement in the $I - V$ characteristics of the diode with the potential well further regraded to the right. It would seem that electrons leave the potential well more easily as the right intrinsic region is graded further towards the anode thus, less charge settle in the potential well. The current density increases with increases in the grading of the potential well on the right intrinsic region thereby, making the diode behavior more ideal. In this way, we estimated and

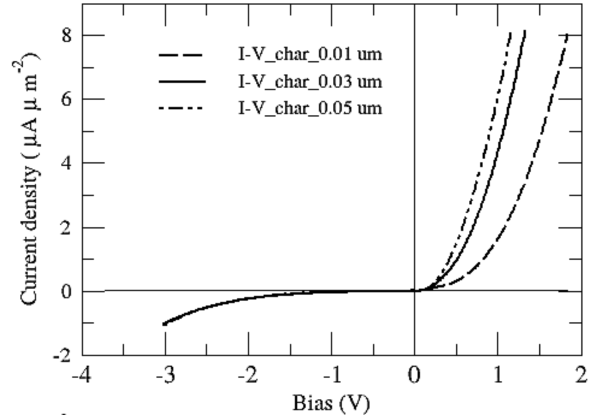

Fig. 2 $I - V$ Characteristics of diodes showing higher currents at all biases as potential well is further regraded on the right intrinsic region

compare the ideality factor, n of the diodes which is a measure of how close a diode is to an ideal diode equation given as:

$$I = I_{sat}\left(e^{\frac{qv}{nkT}} - 1\right) \qquad (1)$$

As shown in the Fig. 2, the ideality factor of the diode improves as the grading of the right intrinsic region increases. It therefore means that any physical effect that increases the ideality factor would substantially impact the saturation current, I_{sat} so that a diode with a high ideality factor would typically have a lower turn on voltage.

The ideality factor as computed using equation 1 was obtained respectively for $0.01, 0.03$ and $0.05\ \mu m$ as 2.76, 1.91 and 1.48. This approaches unity as the edge of the potential well on the right intrinsic region is regraded further to the anode.

Also, as shown in Fig. 2, the turn-on voltage of the diodes was estimated at a current density of $0.5\ \mu A \mu m^{-2}$, the diodes with graded regions of 0.01, 0.03 and 0.05 μm have turn-on voltage of 0.85, 0.5 and 0.38 V respectively.

B. Density of electrons in the potential wells

The density of electrons in the potential well is very important because it determines the barrier height of the diode. The magnitude

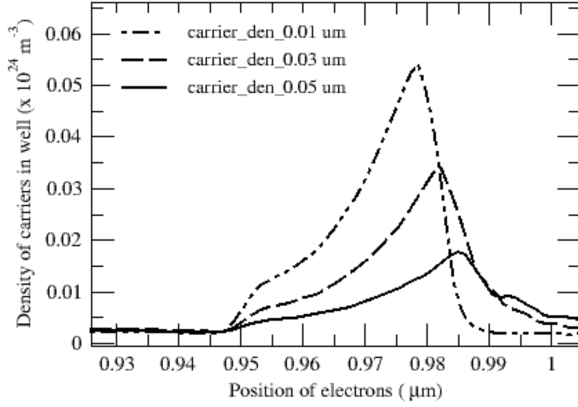

Fig. 3 Electron density in the potential well of the PWB diode for the three well designs.

of the barrier height of a PWB diode depends on how much charge accumulates in the potential well. A low density of charge in the potential well results in a lower barrier height while large amount of charge in the well results in a bigger barrier height. Fig. 3 illustrates the density of electrons in each of the well designs. It can be shown that as the grading of the potential well increases further to the right, the density of electrons in the well reduces. This is because as the well regrades further to the right intrinsic region, electrons leave the potential well faster and more easily to the anode even under influence of low applied bias thus, increasing the current density in the device. As a result, the abrupt heterojunction presented by the diode with graded region of 0.01 μm has the highest turn-on voltage while diode with graded region of 0.05 μm has the lowest turn-on voltage.

C. Electric field behaviour across diode

The electric field of the diodes as estimated from the Monte Carlo model is as shown in Fig. 4. The field of the diode with graded intrinsic region of $0.05\ \mu m$ increases rapidly and is higher than the field of diodes with graded regions of 0.03 and $0.01\ \mu m$ with the latter having the least electric field up to position of approximately $1.0\ \mu m$. This reflects the velocity of charge within the region. Beyond the position of $\sim 1.0\ \mu m$ across the diode however, the electric field increases as the length of the graded intrinsic region decreases.

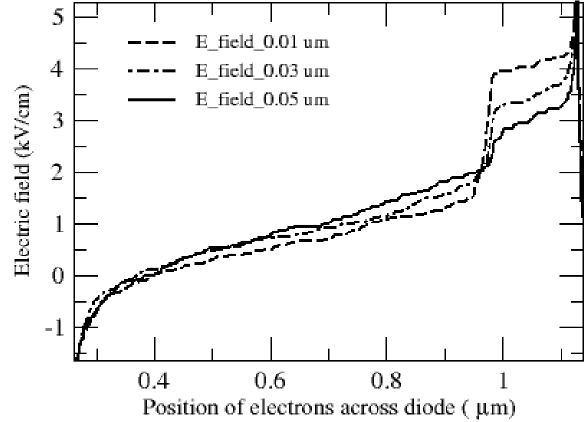

Fig. 4 Electric field distribution across active regions of diode for various shapes of the potential well.

D. Saturation current and curvature coefficient Estimation

The exact on-wafer measurement of the diode's capacitance was estimated using, $C_j \cong A\varepsilon/L$ where A, is the area of diode and L, the length of diode. The capacitance was estimated to be $0.23\ pF$ and the value of the saturation current, I_{sat} for each of the diodes was obtained using the relation [11].

$$\frac{dV}{dI} = \frac{V_o}{I_{sat}} \qquad (2)$$

where $V_o = nkT/q$. The saturation current respectively for diodes with graded regions of 0.01, 0.03 and $0.05\ \mu m$ was estimated to be 0.012×10^{-6}, 0.118×10^{-6} and $0.163 \times 10^{-6}\ A$.

Also, we estimated the curvature coefficient, $(\gamma) = (d^2I/dV^2)/(dI/dV)$ [12] as a measure of diode performance. The curvature coefficient estimated at a bias of $0.3\ V$ for diodes with graded regions of 0.01, 0.03 and $0.05\ \mu m$ respectively was $6.4, 10.3$ and $20.1\ V^{-1}$. The diode with graded region of $0.05\ \mu m$ has the highest curvature coefficient while that with regions of $0.01\ \mu m$ has the least. The result of the

A summary of the dc characteristics of the diodes is as shown in Table 1.

Table 1 Comparison of important dc characteristics

DC quantity	Dimension of regraded well region, μm		
	0.01	***0.03***	***0.05***
Curvature Coefficient, V^{-1}	6.4	10.3	20.1
Ideality factor	2.76	1.91	1.48
Turn-on voltage, V	0.85	0.5	0.38
Saturation current, μA	0.012	0.118	0.163

curvature coefficient is much less compared to that of the ideal Schottky barrier diode with estimated curvature coefficient of $q/kT = 38.6\,V^{-1}$. This result however, compares favorably well with the curvature coefficient reported for GaN Heterostructure barrier diodes with value of $30\,V^{-1}$ [8] and Si-based microwave detector with value of $23.2\,V^{-1}$ [13].

4. Conclusion

The improvements offered to the operation of the PWB diode through redesigning of the potential well has revealed a remarkable dependence of barrier height on design of well. The inconstancy in the $I-V$ characteristics, curvature coefficient turn-on voltage and ideality factor has clearly shown the variations in the potential well design of this diode. This design approach which offers improvement to the performance of PWB diode also suggests some advantages over the Schottky barriers and PDB due to ease of modifying the barrier height.

Acknowledgments. This work is supported by the University of Aberdeen, UK.

References

[1] R.J. Malik, T.R. Aucoin, R.L. Ross, K. Board, C.E.C. Wood and L.F. Eastman, "*Planar doped barriers in GaAs by molecular beam epitaxy*", Electron Lett. **16**(22), pp. 836–838, 1980.

[2] R.J. Malik and S. Dixon, "*A subharmonic mixer using a planar doped barrier dioide with symmetric conductance*", IEEE Electron Dev. Lett. **3**(7), pp. 205–207, July 1982.

[3] M. Akura, G. Dunn, M. Missous and J. Sexton, "*Potential Well Barrier Diodes for submillimeter wave and high frequency applications*", IEEE Electron Dev. Lett. **38**(4), pp. 438–440, April 2017.

[4] M. Akura, G. Dunn, J. Sexton and M. Missous, "*GaAs/AlGaAs potential well barrier diodes: Novel diodes for detector and mixer applications*", Phys. Status Solidi A, **214,** pp. 1700290, July 2017.

[5] M. Akura and G. Dunn, "*Investigating the role of band offset on the property and operation of the Potential Well Barrier diodes*", Phys. Status Solidi B, **256,** pp. 1800284, January 2019.

[6] M. Akura, G. Dunn, and M. Missous, "*Hot electron effect on the operation on the operation of the PWB diode*", J of Semicond. (Accepted for publication)

[7] J.M. Shannon, "*A majority-carrier carmel diode*", Appl. Phys. Lett. **35**(1), pp. 63–65, 1979.

[8] Z. Pei, A. Verma, J. Verma, H. Xing, P. Fay and D. Jena, "*GaN heterostructure barrier diodes exploiting polarization induced-doping*", IEEE Electron Dev. Lett. **35**(6), pp. 615–617, June 2014.

[9] M.J. Kearney, A Condie and I. Dale, "*GaAs planar doped barrier diodes for millimeter wave detector applicatiions*", Electron Lett. **27**(9), pp. 721–722, February 1991.

[10] N. Pilgrim, R. Macpherson, A. Khalid, G. Dunn and D. Cumming, "*Multiple and broad frequency response Gunn diodes*," Semicond. Sci.Technol. **24**(1), pp. 105010 (7pp), August 2009

[11] J.L. Hesler and T. W. Crowe, "*Responsivity and noise measurements of Zero-Bias Schottky diiode detectors*", Int. Symp.Space TetraHertz Techn., Pasadena, March 2007.

[12] V. Radisic, K. Leong, C. Zhang, K.K. Loi and S. Sarkozy, "*Demostration of micro-integrated submillimeter wave pixel*", IEEE Trans. Microwave theory Techn. **61**(8), pp. 2949, August 2013.

[13] S. Y. Park, R. Yu, S. Y. Chung, P. R. Berger, P. E. Thompson and P. Fay, "*Delta-doped Si/SiGe zero-bias backward diodes for micro-wave Detection*", IEEE 65th Annual Dev. Res. Conf. pp. 153 - 154, June 2007.