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Small Signal Modelling of 100 nm GaAs pHEMT Process in the 4 K to 293 K Temperature Range

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***Abstract*— HEMT-based Low Noise Amplifiers (LNAs) are often used as the primary sensing device in microwave/millimeter-wave receiver systems. In noise critical applications, such as radio astronomy, to improve their noise performance, they are cooled to cryogenic temperatures of 20 K and lower. At room temperature, the small signal equivalent circuit (SSEC) of HEMT transistors is well-known and supports LNA design. At low temperatures, however, the circuit model is less representative due to temperature related effects that alter the device current-voltage response. In order to improve the understanding of cryogenic HEMT performance, the SSEC parameters of a commercial 100nm gate length GaAs pHEMT have been extracted across a range of temperatures extending from 4 K to 293 K. The results indicate an unexpectedly complex temperature dependent behavior with variation in the SSEC parameters occurring as the transistor is cooled below 150 K and 15 K. The experimental data and extracted SSEC parameters will support future LNA designs across a range of low temperature operating conditions and help to guide the selection of parameters such as the optimum temperature for operation. In addition, the SSEC can also provide key insights into the operation of HEMT transistors at low temperatures.**

Keywords—GaAs pHEMT, low noise amplifier, small-signal equivalent circuit, temperature dependence

I. Introduction

Pseudomorphic High Electron Mobility Transistors (pHEMTs) are widely used in Low Noise Amplifiers (LNAs) in applications that include telecommunications, radio astronomy instrumentation and quantum computing. While characteristics of high gain and low noise performance are universally required, our primary focus lies in developing cutting-edge radio instruments for radio astronomy applications where minimizing noise is crucial to enhance observational sensitivity. This often involves employing optimized transistor structures that support low noise performance through cryogenic cooling of the receiver that minimizes thermal noise. Indium Phosphide (InP) pHEMTs are the preferred choice for achieving ultra-low noise figures in LNAs operating at microwave, millimetre-wave and submillimetre-wave frequencies, especially at cryogenic operating temperatures. The rising demand for a significant quantity of LNAs (Low Noise Amplifiers) and other components is driven by the increasing use of multiple receiver dishes in observatories, such as the Square Kilometre Array Observatory [1]. Additionally, the adoption of complex receiver architectures like focal plane arrays and phased array feeds further contributes to this need. To meet this growing demand in radio astronomy applications, it becomes imperative to investigate commercially available technologies such as Gallium Arsenide (GaAs) pHEMT technology. This technology allows for cost-effective large-scale manufacturing, making it a viable alternative to InP devices.

In support of the above, accurate Small-Signal Equivalent Circuit (SSEC) models play a vital role in LNA design, the SSEC model for HEMTs is shown in Fig. 1 [2]. Typically, these models are available from the foundry or they can be generated based on transistor measurements. It has been established in previous studies for InP pHEMTs that there are elements of the transistor's SSEC model that have a temperature dependent behaviour [3]. This paper presents an investigation into how the parameters of the SSEC model vary with temperature for a commercially available 100nm gate length GaAs pHEMT process from Win Semiconductors.

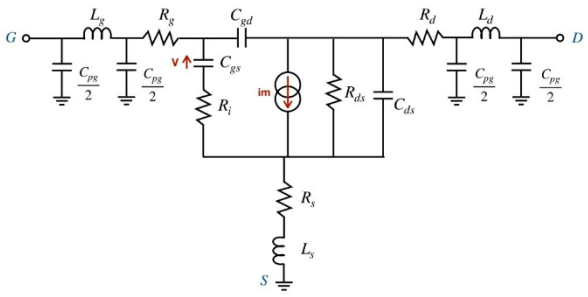

Fig. 1. Small-signal equivalent circuit for modelling the performance of FET and HEMT devices [2]

The measurement system used in this work and details of the measurements are provided in section II. The extracted SSEC extrinsic parameters are shown in section III and the intrinsic parameters provided in section IV along with a comparison of the S-parameters generated from the SSEC model with the measured results.

II. Measurement System

The measurement system is based around a Lakeshore CRX-4K cryogenic probe station that has a temperature range

from 4 K to 293 K (-269.15°C to 19.85°C) with a temperature stability of 50 mK. An on-wafer calibration substrate is included in the probe station to allow the system to be calibrated at the different measurement temperatures. S-Parameters are measured using a Keysight PNA-X N5245A network analyser, and a Keithley 4200-SCS Parameters Analyzer is used to provide bias. Keysight PathWave Device Modelling software (IC-CAP) is used to control the PNA-X and Keithley instruments and to record the measurement results. Fig. 2 illustrates the setup of the measurement system.

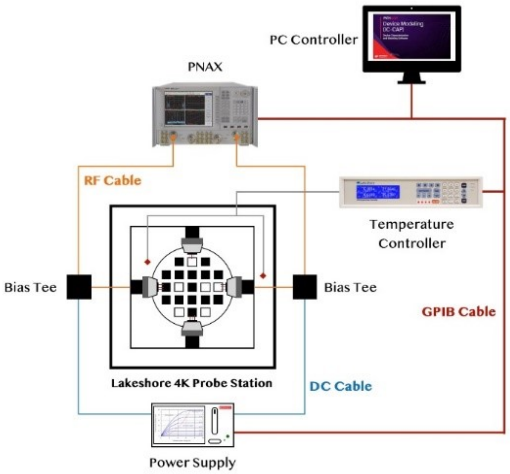

Fig. 2. Block diagram of the cryogenic probe station measurement system. Bias tees are within the PNA-X.

In this study, we conducted measurements of a transistor with 4 gate fingers each with a gate width of 50 µm. The S-Parameters of the transistor have been measured from 100 MHz to 30 GHz with 300 frequency points, at temperature settings of 4 K, 15 K, 77 K, 150 K, 200 K, 250 K and 293 K. Fig. 3 displays the measurement result of S_{21} at 15 GHz and drain current of the bias points used in the extraction of the intrinsic parameters.

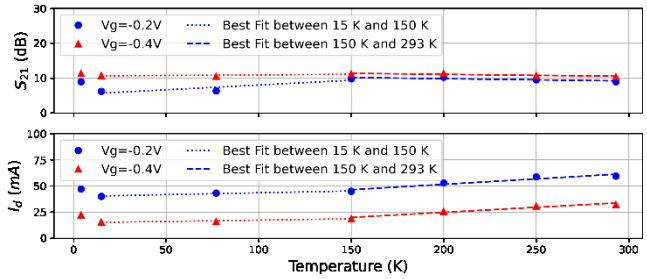

Fig. 3. Measured S_{21} at a frequency of 15 GHz and drain current I_d at V_g = -0.2 V or -0.4 V, and V_d = 0.7 V.

III. SSEC Parameters Extraction

A. *Extrinsic parameters extraction*

The extrinsic values of the SSEC model were extracted using the cold-FET method from [2] [4], the circuit diagram of the SSEC is shown in Fig. 1. The extracted resistor values for the extrinsic SSEC model are presented in Fig. 4 and the capacitor and inductor values in Fig. 5. The extracted inductance and capacitance values exhibit a temperature independent behaviour as expected.

It can be observed from Fig. 4 that the extrinsic resistances of the SSEC display a temperature dependence as the transistor is cooled from room temperature down to 77 K. However, where the values of drain and source resistance (R_d and R_s) plateau as the transistor is cooled below 77 K, the value of the gate resistance (R_g) continues to reduce as the device is cooled to lower temperatures. The behaviour of R_d and R_s is attributed to the properties of the sheet and contact resistances, whereas the change in R_g can be attributed to the increased conductivity obtained by cooling the device to lower temperatures [3].

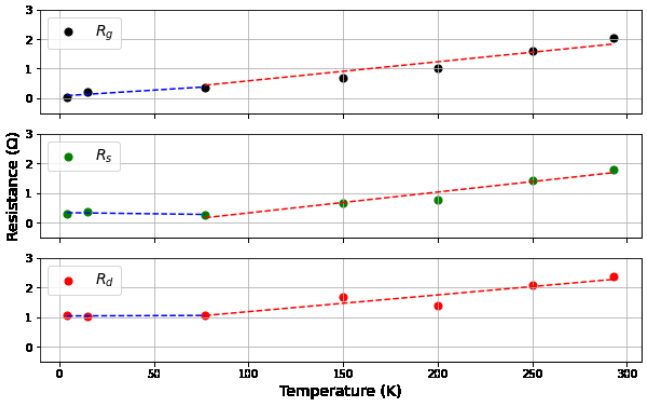

Fig. 4. Gate, source and drain resistance for the extrinsic SSEC model, together with lines of best fit for the ranges 4 K – 77 K and 77 K – 293 K.

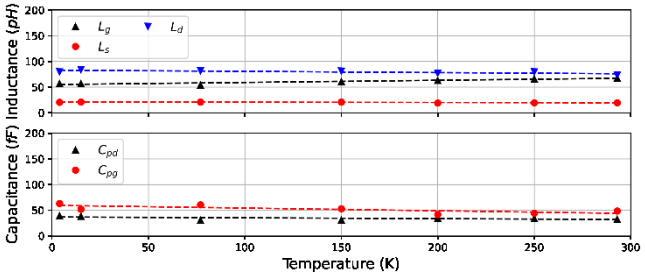

Fig. 5. Gate, source and drain inductance, and gate and drain pad capacitances for the extrinsic SSEC model, together with lines of best fit.

B. *Intrinsic parameters extraction*

The intrinsic SSEC model parameter values have been extracted at bias conditions of V_g = -0.4 V and -0.2 V, and V_d = 0.7 V. The extracted drain-source resistance (R_{ds}) and gate-source resistance (R_{gs}) at the different temperatures are shown in Fig.6, the drain-source capacitance (C_{ds}), gate-drain capacitance (C_{gd}) and gate-source capacitance (C_{gs}) at different temperatures are shown in Fig. 7, and the extracted transconductance (g_m) is shown in Fig. 8.

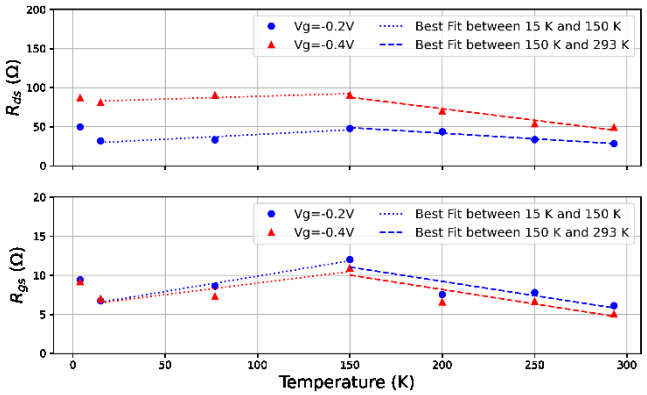

Fig. 6. Extracted drain-source resistance and gate-source resistor values for the intrinsic SSEC model. The biased drain voltage is 0.7 V.

From the results in Fig. 6 and Fig. 7 it can be seen that these gate bias voltages have little effect on any of the intrinsic parameters of the SSEC with the exception of R_{ds}. This would be expected given that higher gate voltages increase the drain current carrying capacity of the transistor.

Finally, the deviation between the measured and modelled S-Parameters results was computed using the equation in [3]. The error for the S_{21} and S_{12} parameters at each temperature was found to be less than 3%, while that of S_{11} and S_{22} was below 8%. The total S parameters error was determined to be no more than 15%. This shows that there is a close match between the measured and the modelled results, showing that the extracted model accurately represents the measured performance of the transistor.

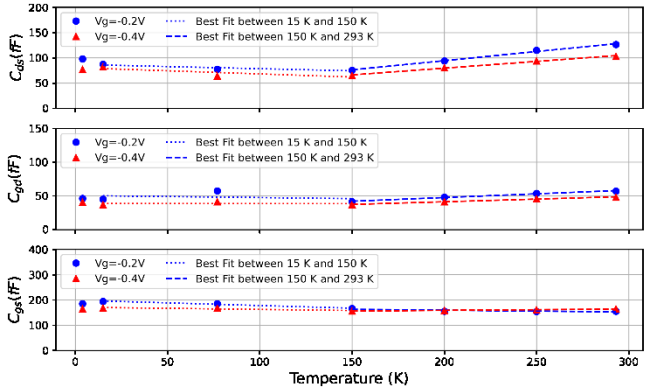

Fig. 7. Extracted drain-source capacitance (C_{ds}), gate-drain capacitance (C_{gd}) and gate-source capacitance (C_{gs}) values for the intrinsic SSEC model.

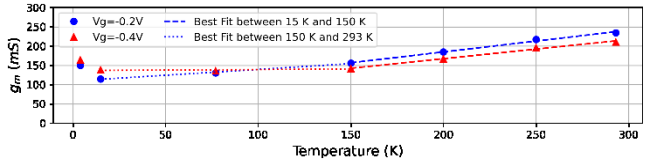

Fig. 8. Extracted transconductance (g_m) values for the intrinsic SSEC model.

IV. Discussion

From the results of the SSEC parameter extraction it can be seen that there is a complex temperature dependent behaviour occurring in the transistor as the operating temperature is reduced. The temperature dependent intrinsic parameters show a distinct change in characteristics when cooled below 150 K and below 15 K. From the Pospieszalski model for transistor noise performance [4], the noise parameter equation for the minimum noise is only dependent on the values of R_{gs} and R_{ds} from the SSEC model. Therefore, the temperature dependent nature of these parameters is something that should warrant further investigation.

The change in behaviour between 15 K and 4 K primarily identifiable in the value of the R_{gs} and to some extent R_{ds}, is likely attributed to the self-heating of the transistor identified in [6]. This change is also visible in the results of [3]. This self-heating effect is caused by the heat generated in the channel of the device being trapped in the gate region of the transistor and preventing any further benefits of cooling the device to lower temperatures. The extraction of the SSEC parameters at these temperatures provides new information to with which the self-heating phenomena can be investigated.

The change of the intrinsic parameters as the device is cooled to temperatures lower than 150K is similarly worth further investigation to see how the behaviour of the elements of the SSEC translates to the performance of the LNA. If the predominant improvement in the performance of the amplifier is seen when cooling to the region of 77K to 150K, with only modest improvements at temperatures below this, then this could allow a new way of utilizing amplifiers within the receiver system. For example, achieving low noise at 77K allows uses of less complex and lower cost cooling system. Correspondingly, where very low temperatures systems are required, e.g. 4 K, the LNAs could be located at a higher temperature within a cryostat, and thus reducing the thermal load on the coldest parts of the system.

V. Conclusions

In this paper we have shown the extraction of the SSEC model component values for a 100 nm gate length GaAs pHEMT at a range of temperatures between 4K and 293K. The values of the extrinsic SSEC components show a complex relationship with temperature but follow the trends that have been shown for InP pHEMTs in [3]. The behaviour of the device needs further investigation in order to establish how the values of the SSEC components relate to the performance of LNAs, including their relation to the noise performance. Of particular interest would be further investigation at temperatures below 150 K and below 15 K in order to investigate the changes in the behaviour of the SSEC parameters identified in this paper. The effects of this could be to offer new approaches for LNAs design and offer new insights into the physics of transistor operation at cryogenic temperatures.

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