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Stability Analysis of Grid-connected VSC-HVDC Systems with Compensated dq Domain Time Delay Models

Shuai Wang
Department of Electrical and Electronic Engineering
The University of Manchester
Manchester, UK
shuai.wang-2@manchester.ac.uk

Robin Preece
Department of Electrical and Electronic Engineering
The University of Manchester
Manchester, UK
robin.preece@manchester.ac.uk

Mike Barnes
Department of Electrical and Electronic Engineering
The University of Manchester
Manchester, UK
mike.barnes@manchester.ac.uk

Abstract—**Voltage Source Converters-based High Voltage Direct Current (VSC-HVDC) transmission systems using Synchronous Reference Frame-Phase-Locked Loops (SRF-PLLs) have been widely studied for modern power systems. The PLL inevitably exhibits a lag in tracking phase angle variation of the power grid voltage. This lag can introduce an equivalent time delay between the controller and systems which may result in potential stability issues. There are also various time delays within converters, which can be simplified into a lumped time delay model applied to the abc domain voltage signals. However, the inaccurate transformation of the time delay model from the abc domain to the dq domain, in which control is typically undertaken, can lead to imprecise representation. An appropriate transformation and its impact on the small-signal stability of SRF-PLL-based VSC-HVDC systems are investigated in this paper. Specifically: a small-signal state-space model of the VSC-HVDC systems is established. A compensation is derived to improve the transformation accuracy of the time delay model into the dq domain. The dq domain impedance and admittance models are then obtained for analysing the stability based on the generalized Nyquist stability criterion. The analysis results from the small-signal model are verified through non-linear time-domain simulations in PSCAD.**

Keywords—Generalized Nyquist stability Criterion (GNC), Synchronous Reference Frame-Phase-Locked Loop (SRF-PLL), Small-signal stability, Time delay model, Voltage Source Converter -High Voltage Direct Current (VSC-HVDC).

I. INTRODUCTION

Voltage Source Converter-based High Voltage Direct Current (VSC-HVDC) transmission technology has been widely utilized in modern power systems [1]. It usually delivers a larger amount of power over a long distance compared to an Alternating Current (AC) transmission line. In practical engineering, various factors, such as physical constraints, communication issues, measurement delays, etc., can result in time delays in the VSC-HVDC system. These delays could deteriorate the system stability and consequently the efficiency of power delivery. Thus, the impact of time delay effects on the stability of the VSC-HVDC systems connected to AC grids should be further investigated.

The Phase-Locked Loop (PLL) is a key component of the present grid-following control-based VSC-HVDC systems. It is used to measure the frequency and phase angle of the interfaced AC systems. The real-time phase angle detected by the PLL will be used by the controller to synchronize the VSC with the AC systems. However, due to its inherent bandwidth limitations, the PLL cannot instantaneously track variations in the power grid voltage. Consequently, there exists a lag between the phase angle employed in the controllers and the actual phase angle in the systems [2,3]. This can slow down the controller's response to system behaviour and potentially lead to instability issues [4]. The lag introduced by the PLL can be equivalently viewed as a time delay between the voltage seen by VSC-HVDC control and the actual power grid voltage. The Synchronous Reference Frame-PLL (SRF-PLL) is the fundamental form of commonly used PLLs in the power industry and thus forms the basis of the study in this paper.

There are additional inherent time delays within converters apart from the equivalent delay associated with the PLLs [1]. Various factors such as calculations, communication, and PWM delays within converters unavoidably lead to a lag between the actual converter voltage outputs and the reference signals. This lagging phenomenon can be characterized by introducing a time delay model between these signals. The time delay can be simplified into a lumped model, incorporating all delays throughout the system into a single value. In converter systems, voltage reference signals are commonly generated in the dq domain and subsequently transformed into three-phase abc domain reference signals using the phase angle of the PLL. As a result, in non-linear time-domain models of converter systems, time delay models can be incorporated into the system through two primary approaches: within the dq domain signals or within the abc domain signals.

The stability analysis of a three-phase electric power system with dq domain controllers often involves its mathematical modelling in the dq domain. The appropriate transformation of three-phase abc domain quantities and their functions into the dq domain (and back again) is therefore required. This issue is often neglected [5]. Some literature embeds time delay models directly into the dq domain signals so the transformation issue is avoided [6,7]. In contrast, others represent the system with time delay models within the abc domain signals while neglecting the necessity of the time delay model transformation from the abc

domain to the dq domain [8]. This can potentially introduce inaccuracies into the analysis results. Hence, an accurate transformation should be investigated. The impact of an inaccurate transformation on the stability analysis results should also be explored.

Therefore, this paper aims to investigating the small-signal stability of VSC-HVDC systems with SRF-PLL and explores the accurate transformation of time delay models within the abc domain signals into the dq domain. The main contributions of this paper are as follows:

1) The development of a dq domain small-signal state-space model for an SRF-PLL based grid-connected VSC-HVDC system.

2) The introduction of a phase compensation matrix to enhance the accuracy of the time delay model transformation from the abc to dq domain.

3) Analysis on the impact of the time delay on the stability of grid-connected VSC-HVDC systems using the models introduced.

The rest of the paper is organized as follows. Section II presents the small-signal modelling of grid-connected VSC-HVDC systems and the stability analysis method. Section III details the compensation for the time delay model transformation from the abc to dq domain. Section IV shows the simulations to verify the analysis results. Finally, section V concludes this paper.

II. SYSTEM DESCRIPTIONS AND MODELLING OF GRID-CONNECTED VSC-HVDC SYSTEMS

A simplified diagram of a VSC-HVDC system connected to a power grid is illustrated in Fig. 1 [9]. The system parameters can be found in Table 1. The system is used to investigate the impact of time delay and SRF-PLL on the small-signal stability of grid-connected VSC-HVDC systems. The power grid is represented as a Thevenin model with an ideal voltage source behind an grid impedance [10]. The VSC is simplified as a controllable voltage source [11]. In the diagram, $v_{c,abc}$, v_{abc}, and $v_{g,abc}$ denotes the three-phase voltages of the converter, the Point of Common Coupling (PCC), and the ideal power grid, respectively. R and L represent the combined equivalent series resistance and inductance of the VSC and transformer. R_g and L_g stand for the resistance and inductance of the power grid, respectively. The control system consists of the inner dq domain decoupling current control loops with PCC voltage proportional feed-forward compensation and SRF-PLL. The topology of the employed SRF-PLL is depicted in Fig. 2. The detected phase angle θ of the PLL is utilized for the Park transform and its inverse for the controller variables. All the variables in the system diagram between the Park transform and its inverse are related to the PLL angle θ. They are denoted with the superscript 'c'. Otherwise, the variables are associated with the actual PCC voltage phase angle θ_{PCC}.

The complete small-signal state-space model of the VSC-HVDC system includes four sub-modules, namely, the inner current control loops with Proportional Integral (PI) controller, time delay elements, converter reactors, and the SRF-PLL.
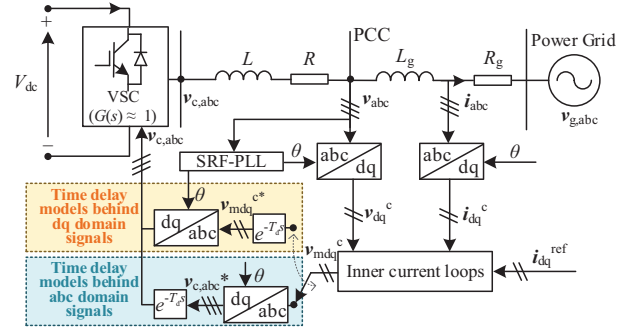

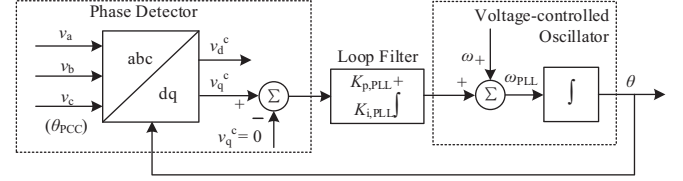Figure 1. Topology of a VSC-HVDC connected to an infinite power grid through a transmission line.

Figure 2. Toplogy of the employed SRF-PLL.

Table 1. Parameters of the MMC-HVDC system.

Parameters	Values
MMC Power rating P	1000 MW
DC voltage V_{dc}	±320 kV
Converter reactor L	0.2 pu
Converter resistance R	0.008 pu
Proportional gain of current loops $K_{p,i}$	1.3 pu
Integral gain of current loops $K_{i,i}$	16.5 pu
Proportional gain of SRF-PLL $K_{p,PLL}$	1.6 pu
Integral gain of SRF-PLL $K_{i,PLL}$	28.9 pu

The internal delay effect of the VSC has been integrated to the time delay model so the transfer function of the VSC is simplified as a unit function. Each sub-module is modelled independently and combined afterwards using the Component Connection Method (CCM) [12]. The generic small-signal state-space model can be expressed as (1).

$$\Delta \dot{x} = A\Delta x + B\Delta u$$
$$\Delta y = C\Delta x + D\Delta u \tag{1}$$

where the symbol Δ denotes the small-signal perturbation; A, B, C, and D are the system matrices which are unique for each submodule and determined by the system parameters. The system matrices of the inner current loops A_i-D_i, converter reactors $A_{reactor}$-$D_{reactor}$, the SRF-PLL A_{PLL}-D_{PLL}, and the power grid A_{grid}-D_{grid} are shown as follows:

$$A_i = \mathbf{0}_{2\times 2},\ B_i = [1, 0; 0, 1], \tag{2}$$
$$C_i = [K_{i,i}, 0; 0, K_{i,i}],\ D_i = [K_{p,i}, 0; 0, K_{p,i}].$$

$$A_{reactor} = [-R/L, \omega; -\omega, -R/L],$$
$$B_{reactor} = [1/L, 0, -1/L, 0; 0, 1/L, 0, -1/L], \tag{3}$$
$$C_{reactor} = [1, 0; 0, 1],\ D_{reactor} = \mathbf{0}_{2\times 4}$$

$$A_{PLL} = [0, K_{i,PLL}; 0, 0],\ B_{PLL} = [K_{p,PLL}; 1],\ C_{PLL} \tag{4}$$
$$= [1, 0],\ D_{PLL} = 0$$

$$\boldsymbol{A}_{\text{grid}} = [-R_{\text{g}}/L_{\text{g}}, \omega; -\omega, -R_{\text{g}}/L_{\text{g}}],$$
$$\boldsymbol{B}_{\text{grid}} = [1/L_{\text{g}}, 0, -1/L_{\text{g}}, 0; 0, 1/L_{\text{g}}, 0, -1/L_{\text{g}}], \quad (5)$$
$$\boldsymbol{C}_{\text{grid}} = \boldsymbol{I}_{2\times2}, \boldsymbol{D}_{\text{grid}} = \boldsymbol{0}_{2\times4}.$$

where $K_{\text{i,i}}$ and $K_{\text{p,i}}$ are the integral gain and proportional gain of the current-loops PI controller, respectively; ω is the system nominal angular frequency; $K_{\text{i,PLL}}$ and $K_{\text{p,PLL}}$ are integral and proportional gains of PI controller respectively. The system matrices $\boldsymbol{A}_{\text{del}}$, $\boldsymbol{B}_{\text{del}}$, $\boldsymbol{C}_{\text{del}}$, $\boldsymbol{D}_{\text{del}}$ of the time delay model can be derived from the linearized time delay model in (6).

$$G_{\text{del}}(s) = e^{-T_{\text{d}}s} \approx \frac{60 - 24T_{\text{d}}s + 3T_{\text{d}}^2s^2}{60 + 36T_{\text{d}}s + 9T_{\text{d}}^2s^2 + T_{\text{d}}^3s^3} \quad (6)$$

where T_{d} is the delayed time.

The input and output vectors of the VSC-HVDC system are defined as $\boldsymbol{u}_{\text{VSC}} = [i_{\text{d}}^{\text{ref}}, i_{\text{q}}^{\text{ref}}, v_{\text{d}}, v_{\text{q}}]^T$ and $\boldsymbol{y}_{\text{VSC}} = [i_{\text{d}}, i_{\text{q}}]^T$ respectively, where $i_{\text{d}}^{\text{ref}}$ and $i_{\text{q}}^{\text{ref}}$ are the output currents references. The input and output vectors of the power grid are defined as $\boldsymbol{u}_{\text{grid}} = [v_{\text{d}}, v_{\text{q}}, v_{\text{gd}}, v_{\text{gq}}]^T$ and $\boldsymbol{y}_{\text{grid}} = [i_{\text{d}}, i_{\text{q}}]^T$ respectively, where v_{gd} and v_{gq} are the power grid d- and q-axis voltages. Thus, the dq domain impedance and admittance matrices $\boldsymbol{Z}_{\text{dq}}$ and $\boldsymbol{Y}_{\text{dq}}$ can be calculated with the transfer functions of the division of the input and output: $\boldsymbol{Z}_{\text{dq}} = \boldsymbol{v}_{\text{dq}}/\boldsymbol{i}_{\text{dq}}$ and $\boldsymbol{Y}_{\text{dq}} = \boldsymbol{i}_{\text{dq}}/\boldsymbol{v}_{\text{dq}}$. The converter admittance and power grid impedance are denoted as $\boldsymbol{Y}_{\text{con}}$ and $\boldsymbol{Z}_{\text{grid}}(s)$, respectively. The impedance-based Generalized Nyquist stability Criterion (GNC) is used to analyse the stability [13]. The stability of the system can be examined by checking the Nyquist plots of the characteristic values of the minor loop matrix $\boldsymbol{Z}_{\text{grid}}\boldsymbol{Y}_{\text{con}}$ [14]. If the plots do not encircle the point $(-1, 0)$ in the complex plane, then the system is deemed stable [15].

III. ACCURACY COMPENSATION FOR THE TIME DELAY MODEL TRANSFORMATION FROM THE abc TO dq DOMAIN

The time delay effect is simplified into a lumped model $G_{\text{del}}(s)$ in (6), in which all delays throughout the system are incorporated into a single value. The majority of the potentially harmful delays exist within the converter [1] so it is preferable to place the lumped delay model $G_{\text{del}}(s)$ between the voltage reference signals and actual output voltages. Two potential placements of the time delay model have been considered and discussed, as depicted in Fig. 1. The first placement is that the time delay models are integrated within the dq domain voltage signals, i.e., behind the dq domain converter voltage reference signals $\boldsymbol{v}_{\text{mdq}}^{\text{c}}$. Another option is that the time delay models are integrated within the abc domain voltage signals, i.e., behind the abc domain converter voltage reference signals $\boldsymbol{v}_{\text{c,abc}}^{*}$ (i.e., v_{ca}^{*}, v_{cb}^{*}, and v_{cc}^{*}). It is worth noting that both configurations are simplified ways to incorporate the time delay into the overall system model. As discussed earlier, the system small-signal model needs to be constructed in the dq domain. The abc domain quantities and their relationships are required to be transformed into the dq domain. When time delay models are integrated within the dq domain voltage signals, additional transforms are not needed for the time delay models. However, an accurate
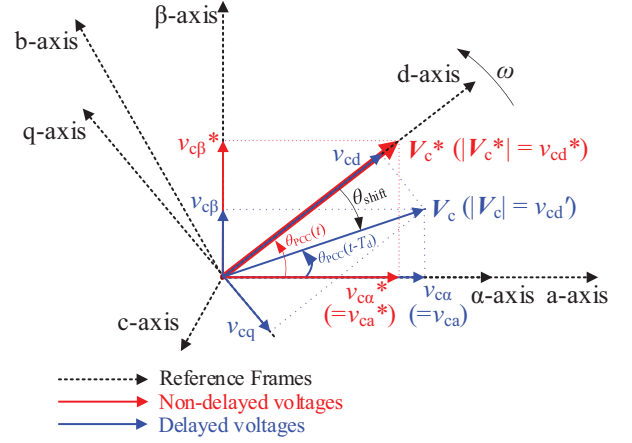

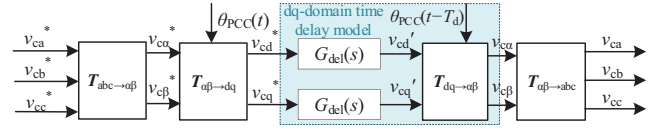Figure 3. The Reference Frames.

Figure 4. The dq domain time delay model with the correct phase angle for the inverse Park transform.
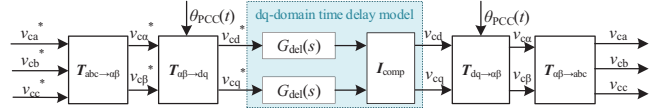

Figure 5. The dq domain time delay model with the compensation and αβ-abc transform.

transformation is necessary when time delay models are integrated within the abc domain voltage signals behind $\boldsymbol{v}_{\text{c,abc}}^{*}$.

The discrepancy between the time delay model in the abc signals and its model in the dq domain can be clarified by analysing the time delay model in the reference frames in Fig. 3. V_{c}^{*} represents the non-delayed rotating voltage vector $\boldsymbol{v}_{\text{c,abc}}^{*}$. The time delay model functions by clockwise rotating V_{c}^{*} to a delayed rotating voltage vector V_{c}. For simplicity, V_{c}^{*} is assumed to align with the d-axis so its projection on the d-axis v_{cd}^{*} remains identical to its modulus value $|V_{\text{c}}^{*}|$. All those variables are associated with the actual PCC voltage phase angle θ_{PCC}. Thus, the actual real-time phase angle between the d-axis and a-axis $\theta_{\text{PCC}}(t)$ is used for the Park transform $\boldsymbol{T}_{\alpha\beta\rightarrow\text{dq}}$. The time delay model $G_{\text{del}}(s)$ is embedded into each phase sinusoidal signal. Through Fig. 3, this represents the projection of the delayed rotating voltage vector V_{c} onto the a-, b-, and c-axes. The abc domain is a stationary coordinate system that keeps fixed when the voltage vector experiences delays. Thus, the projections of the delayed rotating voltage vector on each axis capture the delay effect. The αβ domain is also a stationary coordinate system. Thus, the time delay model in the abc domain time delay model can be interchanged with that in the αβ domain.

However, the dq domain is a rotating coordinate system, transforming components into signals along the d- and q-axes. From Fig. 3, when implementing $G_{\text{del}}(s)$ for d- and q-axis

components independently, the delayed voltage v_{cd}' remains positioned at the original location of the rotating voltage vector V_c^*, rather than the delayed rotating voltage vector V_c. To address this, v_{cd}' requires an additional clockwise rotation to align with the position of V_c, where the real-time phase angle between the v_{cd}' and a-axis represents the angle of the voltage at the delayed time T_d ago, denoted as $\theta_{PCC}(t - T_d)$, rather than $\theta_{PCC}(t)$. If $\theta_{PCC}(t)$ remains for the inverse Park transform, the resultant dq domain model will exhibit greater stability than the abc domain model as the time delay effect is reduced. As a solution, the delayed real-time phase angle $\theta_{PCC}(t - T_d)$ can be employed for the inverse transform, as shown in Fig. 4, i.e., to project v_{cd}' on the $\alpha\beta$ domain at the position of V_c. This compensation can address the inaccuracy of the dq domain time delay model.

Based on the reference frames in Fig. 3 and the time delay model in Fig. 4, the mathematical relationship can be derived as follows. The dq domain variables vectors are expressed as $\boldsymbol{v}_{cdq}^* = [v_{cd}^*; v_{cq}^*]$, $\boldsymbol{v}_{cdq}' = [v_{cd}'; v_{cq}']$ and $\boldsymbol{v}_{cdq} = [v_{cd}; v_{cq}]$. The $\alpha\beta$ domain variables vectors are expressed as $\boldsymbol{v}_{c\alpha\beta}^* = [v_{c\alpha}^*; v_{c\beta}^*]$ and $\boldsymbol{v}_{c\alpha\beta} = [v_{c\alpha}; v_{c\beta}]$. The Park transform between $\boldsymbol{v}_{cdq}^*$ and $\boldsymbol{v}_{c\alpha\beta}^*$ in Fig. 4 can be expressed in (7).

$$\boldsymbol{v}_{cdq}^* = e^{-j\theta_{PCC}(t)}\boldsymbol{v}_{c\alpha\beta}^* \tag{7}$$

The dq domain time delay model between $\boldsymbol{v}_{cdq}'$ and $\boldsymbol{v}_{cdq}^*$ is shown in (8).

$$\boldsymbol{v}_{cdq}' = G_{del}\boldsymbol{v}_{cdq}^* \tag{8}$$

The inverse Park transform from $\boldsymbol{v}_{c\alpha\beta}$ to $\boldsymbol{v}_{cdq}'$ with the delayed phase angle is shown in (9).

$$\boldsymbol{v}_{c\alpha\beta} = e^{j\theta_{PCC}(t-T_d)}\boldsymbol{v}_{cdq}' \tag{9}$$

So, if the delayed phase angle $\theta_{PCC}(t - T_d)$ is used for the inverse Park transform, the output-input relationship between $\boldsymbol{v}_{c\alpha\beta}$ and $\boldsymbol{v}_{c\alpha\beta}^*$ in Fig. 4 is deduced as follows in (10).

$$\boldsymbol{v}_{c\alpha\beta} = e^{j[\theta_{PCC}(t-T_d)-\theta_{PCC}(t)]}G_{del}\boldsymbol{v}_{c\alpha\beta}^* \tag{10}$$

Therefore, employing the delayed phase angle for the inverse Park transform can rectify the inaccuracy of the dq domain time delay model. However, all variables in the same dq domain model must be aligned with same reference frame and a uniform phase angle. This can be achieved by adding a phase compensation factor $\boldsymbol{I}_{comp}$ to account for the impact of the delayed phase angle on the inverse Park transform, while preserving the use of the non-delayed phase angle for the inverse Park transform, as depicted in Fig. 5. The aim is to make the two models in Fig. 4 and Fig. 5 functionally equivalent. That is, to derive the phase compensation factor $\boldsymbol{I}_{comp}$ so that the outputs in both models are the same. The relationship between $\boldsymbol{v}_{c\alpha\beta}$ and $\boldsymbol{v}_{c\alpha\beta}^*$ in Fig. 5 is shown in (11).

$$\boldsymbol{v}_{c\alpha\beta} = G_{del}\boldsymbol{I}_{comp}\boldsymbol{v}_{c\alpha\beta}^* \tag{11}$$

Compared (10) and (11), the phase compensated factor $\boldsymbol{I}_{comp}$ can be obtained in (12).

$$\boldsymbol{I}_{comp} = e^{j[\theta_{PCC}(t-T_d)-\theta_{PCC}(t)]} = e^{j\theta_{shift}} \tag{12}$$

The phase compensation factor $\boldsymbol{I}_{comp}$ is a non-linear function which needs to be linearised for the small-signal modelling. Two assumptions are made for the linearization: 1) The ideal time delay e^{-sT_d} is considered and 2) Only the phase angle shift at fundamental angular frequency ω is considered. With the two assumptions, the shifted angle θ_{shift} can be calculated by the multiplication of the time delay and angular frequency. This gives (13).

$$\theta_{shift} = \theta_{PCC}(t - T_d) - \theta_{PCC}(t) \approx -\omega \cdot T_d \tag{13}$$

The phase compensation factor $\boldsymbol{I}_{comp}$ in (12) can be expressed in matrix form and further linearised based on (13), as shown in (14).

$$\boldsymbol{I}_{comp} = \begin{bmatrix} \cos(\omega T_d) & \sin(\omega T_d) \\ -\sin(\omega T_d) & \cos(\omega T_d) \end{bmatrix} \tag{14}$$

With (14) as the phase compensation matrix for the dq domain time delay model, the inaccuracy caused by the transformation of the time delay model from the abc domain to dq domain can be improved.

IV. SIMULATION VERIFICATION

The system depicted in Fig. 1 with the data detailed in Table 1 is used to analyse the impact of the time delay model on the stability of the grid-connected VSC-HVDC systems with an SRF-PLL. Based on the built dq domain small-signal model and the impedance-based GNC, the instability boundary of the time delay value across various strengths of the power grid is calculated for the time delay models integrated within the dq and abc domain signals respectively. The strength of the connected power grid is quantified by the Short Circuit Ratio (SCR), which is defined as the ratio of the short circuit capacity of the power grid to the rated power of the connected VSC-HVDC systems. Furthermore, the accuracy improvement of the stability analysis with the compensated dq domain time delay model is also studied. For verification, all analysis results from the small-signal model are compared with the non-linear time-domain Electromagnetic Transient (EMT) simulation in PSCAD. The EMT model is based on the system with inner dq domain current control loops in Fig. 1. The VSC is modelled as a controllable voltage source ignoring high frequency harmonics.

When the time delay model is directly integrated within the dq domain signals, the time delay stability boundaries versus SCR are presented in Fig. 6. When the time delay exceeds the boundaries, the system will become unstable. It can be observed that the results from the small-signal model and non-linear EMT simulation match well as a whole. Specifically, when the SCR is greater than around 7.5, the time delay boundaries are fixed at around 0.743 ms and 0.78 ms for the small-signal model and
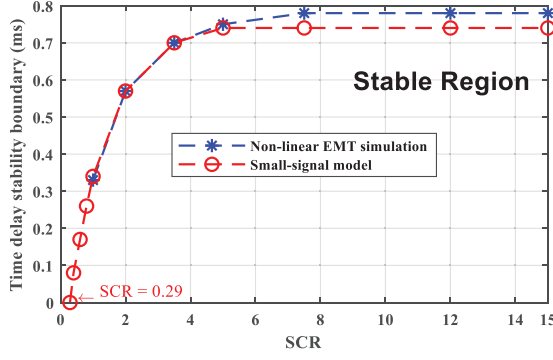
Figure 6. Time delay stability boundary versus SCR with the time delay model within the dq domain siganls: Results comparsion of the Non-linear EMT simulation and small signal model.
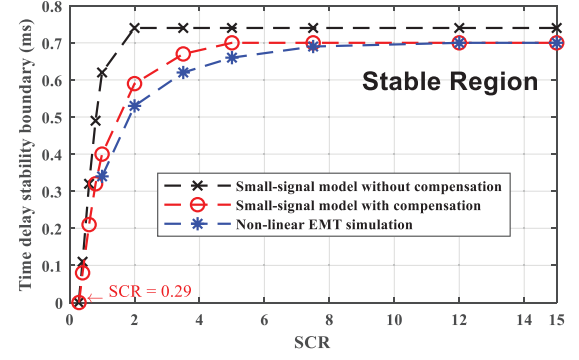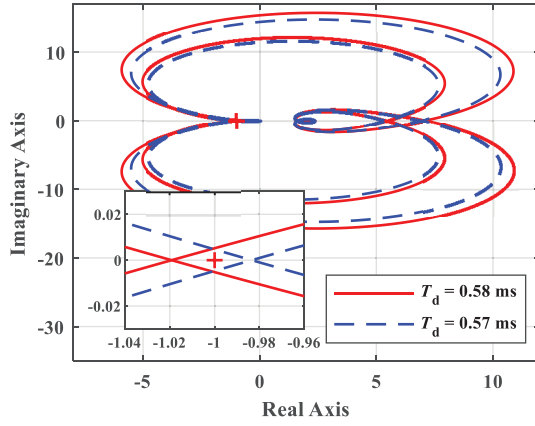

Figure 7. The Nyquist curves for $T_d = 0.57$ ms and $T_d = 0.58$ ms with the time delay model within the dq domain signals when SCR = 2.0.
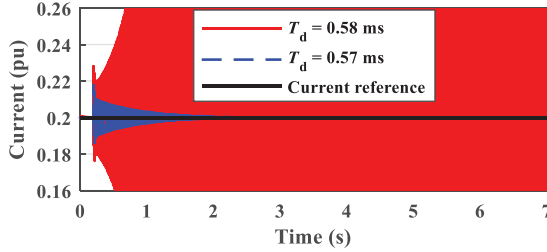

Figure 8. The d-axis current time-domain EMT simulation results for $T_d = 0.57$ ms and $T_d = 0.58$ ms with the time delay model within the dq domain signals when SCR = 2.0.

EMT simulation respectively. The small-signal model outcomes emphasize that the time delay within the converter considered here must not exceed 0.743 ms in any scenario even when the VSC is connected to an infinite power grid. In addition, the tolerance for the time delay value reduces as the SCR decreases. When the SCR is lower than 0.2, the VSC will not withstand any level of time delay within the system. Therefore, it is crucial to minimize the time delay within the converter to be as small as the conditions allow to ensure stability when the VSC-HVDC is connected to a weak power grid.

Fig. 7 displays the Nyquist curves with the time delay model within the dq domain signals when the SCR is 2.0. The plots
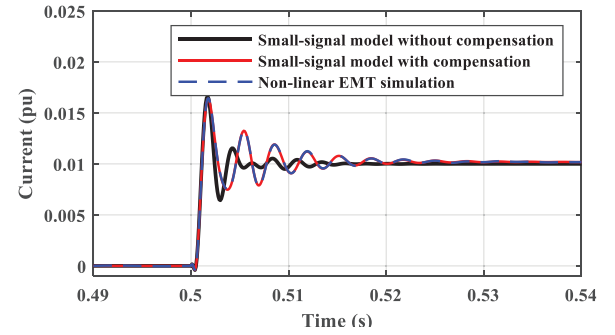

Figure 9. Time delay stability boundary versus SCR with the time delay model within the abc domain signals: Results comparsion of the Non-linear EMT simulation and small signal models with/without compensation for the dq domain time delay model.

Figure 10. The d-axis current step change responses when the SCR is infinite: Results comparsion of the Non-linear EMT simulation and small signal model with/without compensation for the dq domain time delay model.

demonstrate that the Nyquist plots encircle the point $(-1, 0)$ for $T_d = 0.58$ ms, indicating that the system is unstable, while they do not for $T_d = 0.57$ ms. Thus, the stability boundary of time delay as per the GNC is determined to be 0.57 ms. To corroborate the small-signal analysis results, the time-domain EMT simulation results are shown in Fig. 8. At 0.2 s, T_d is altered to different values from a stable operating point. The current response exhibits damped oscillations for $T_d = 0.57$ ms whereas it demonstrates growing oscillations for $T_d = 0.58$ ms. The EMT simulation results prove the accuracy of the small-small model. The time delay stability boundaries versus SCR when the time delay model is within the abc domain signals are presented in Fig. 9. When the compensation is not considered for the dq domain time delay model, it is evident that the results of the stability boundaries between the small-signal model and EMT simulation have substantial discrepancies. In contrast, the results from the small-signal model considering the time delay model compensation shows better alignment with the EMT results, particularly when the SCR is no lower than 12.0. When the SCR is below 12.0, there are still discrepancies of the stability boundaries between the small-signal model and EMT simulation, but they remain within acceptable engineering requirements if a 20% tolerance margin is considered. The discrepancies are mainly because the compensation matrix uses the nominal system angular frequency ω_0. In reality, when the
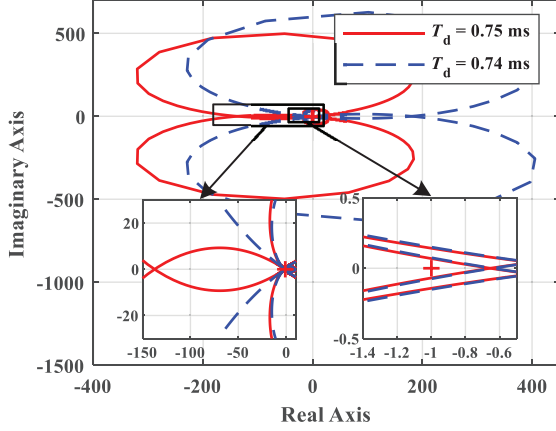
Figure 11. The Nyquist curves for $T_d = 0.74$ ms and $T_d = 0.75$ ms with the time delay model within the abc domain signals when SCR = 2.0: small signal model without compensation for the dq domain time delay model.
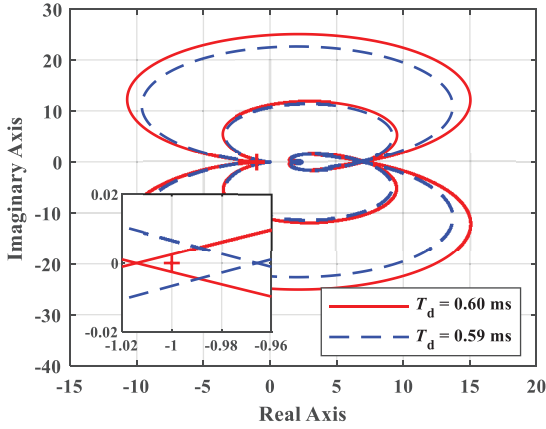

Figure 12. The Nyquist curves for $T_d = 0.59$ ms and $T_d = 0.60$ ms with the time delay model within the abc domain signals when SCR = 2.0: small signal model with compensation for the dq domain time delay model.

SCR is relatively lower, the power grid voltage will be more volatile and the actual frequency will vary around ω_0. As a result, the accuracy of the compensation for the time delay model will be compromised but it remains useful when the power grid is weak. On the other hand, the results indicate that the compensation can improve the accuracy of the time delay model very well when the SCR is high. This explains the better alignment of the time delay stability boundary results from the small-signal model with compensation and the EMT simulation when the SCR is greater than 12.0. The substantial improvement of the compensation for the time delay model under a higher SCR condition can be also illustrated by examining the time-domain current step responses of the small-signal model and the EMT simulation. A comparison of step responses for infinite SCR is shown in Fig. 10. It can be seen that compared to the small-signal model without compensation, the curve of current step responses of the small-signal model with the compensation can match very well with the non-linear EMT simulation results. Thus, the phase compensation matrix is an effective method to improve the accuracy of the dq domain time delay model.
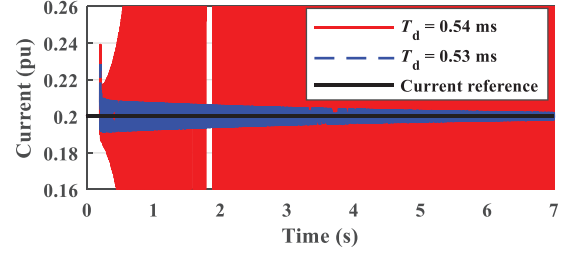

Figure 13. The d-axis current time-domain EMT simulation results for $T_d = 0.53$ ms and $T_d = 0.54$ ms with the time delay model within the abc domain signals when SCR = 2.0.

The Nyquist curves with the time delay model on the abc domain side with the SCR being 2.0 are illustrated in Fig. 11 and Fig. 12. From Fig. 11 for the time delay model without compensation, the plots demonstrate that the Nyquist plots encircle the point (−1, 0) for $T_d = 0.75$ ms, indicating that the system is unstable, while they do not for $T_d = 0.74$ ms. Thus, the stability boundary of time delay when the dq domain time delay model is not compensated is 0.74 ms. From Fig. 12 for the time delay model with compensation, the stability boundary of time delay when the dq domain time delay model is improved is 0.59 ms. To verify the small-signal analysis results, the time-domain EMT simulation results are shown in Fig. 13. At 0.2 s, T_d is changed to different values from a stable operating point. The current response exhibits damped oscillations for $T_d = 0.53$ ms while shows growing oscillation for 0.54 ms. The stability boundary obtained from the EMT simulation is 0.53 ms. With this SCR value of 2.0, the error of the model with compensated time delay model is 11% while the error of the model without compensated time delay model is 40%. The results comparison between the small-signal models and non-linear EMT simulation proves the effectiveness of the compensated dq domain time delay model.

V. CONCLUSIONS

A small-signal state-space model of a VSC-HVDC system was developed. An impedance-based Generalized Nyquist stability Criterion has been used to analyse the stability of the VSC-HVDC system connected to a power grid. The investigation was focused on assessing the impact of time delay on system stability. It was found that an around 0.7 ms time delay within the converters considered in this paper represents the maximum tolerable time delay value by the VSCs. When the VSC is connected to a weaker power grid, the permittable time delay will be reduced. Any time delay is not expected to ensure the system stability when the power grid is too weak or the SCR is below a certain value. In addition, a phase compensation factor is needed when transforming the time delay models in the abc domains signals into the dq domain. The compensation can effectively improve the accuracy of the stability analysis results if the time delay model is included in the dq domain small-signal models.

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