MANCHESTER 1824
The University of Manchester

The University of Manchester Research

Complementary Integrated Circuits Based on p-Type SnO and n-Type IGZO Thin-Film Transistors

DOI:
10.1109/LED.2017.2786237

Document Version
Accepted author manuscript

Link to publication record in Manchester Research Explorer

Citation for published version (APA):
Li, Y., Yang, J., Wang, Y., Ma, P., Yuan, Y., Zhang, J., Lin, Z., Zhou, L., Xin, Q., & Song, A. (2018). Complementary Integrated Circuits Based on p-Type SnO and n-Type IGZO Thin-Film Transistors. *IEEE Electron Device Letters*, *39*(2), 208 - 211. https://doi.org/10.1109/LED.2017.2786237

Published in:
IEEE Electron Device Letters

Citing this paper
Please note that where the full-text provided on Manchester Research Explorer is the Author Accepted Manuscript or Proof version this may differ from the final Published version. If citing, it is advised that you check and use the publisher's definitive version.

General rights
Copyright and moral rights for the publications made accessible in the Research Explorer are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

Takedown policy
If you believe that this document breaches copyright please refer to the University of Manchester's Takedown Procedures [http://man.ac.uk/04Y6Bo] or contact openresearch@manchester.ac.uk providing relevant details, so we can investigate your claim.

Download date:24. May. 2025

Complementary Integrated Circuits Based on p-type SnO and n-type IGZO Thin-Film Transistors

Yunpeng Li, Jin Yang, Yiming Wang, Pengfei Ma, Yvzhuo Yuan, Jiawei Zhang, Zhaojun Lin, Li Zhou, Qian Xin, and Aimin Song, *Senior Member, IEEE*

***Abstract*—Oxide semiconductors are highly attractive for the new-generation transparent/flexible electronics. In this letter, logic gates (inverter, NAND and transmission gates) and 3-stage ring oscillators based on n-type indium-gallium-zinc-oxide (IGZO) thin-film transistors (TFTs) and p-type tin monoxide (SnO) TFTs are presented. The IGZO TFTs show a mobility of 10.05 cm^2/(V·s) and a threshold voltage of 5.00 V. The SnO TFTs exhibit a mobility of 1.19 cm^2/(V·s) and a matched threshold voltage of -5.05 V. At a supply voltage of 10 V, the complementary inverters show an extremely high gain of 112 with a geometric aspect ratio of 5. The dynamic responses of the logic gates based on n-type IGZO and p-type SnO TFTs are also examined. The delay time of the inverter measured from dynamic response is 27.75 µs at a supply voltage of 10 V. The inverter, NAND, and transmission gates all exhibit ideal rail-to-rail output voltage behavior. At a supply voltage of 20 V, the 3-stage ring oscillators are able to operate at 32.87 kHz, and the stage delay is 5.07 µs.**

***Index Terms*— Complementary inverter, logic gates, ring oscillator, tin monoxide (SnO), indium-gallium-zinc-oxide (IGZO), thin-film transistor (TFT).**

I. Introduction

OXIDE semiconductors have received much attention due to a number of advantages including low cost, low fabrication temperatures, high carrier mobilities, good transparency in visible region, mechanical flexibility, as well as scalable deposition methods compared with amorphous silicon[1-4]. Under the advantages mentioned above, oxide semiconductors have been regarded as one of the most promising candidates for transparent/flexible electronics[2, 3].

So far, n-type oxides, such as indium-gallium-zinc-oxide (IGZO), are highly researched and even some of them have been commercialized [4]. For instance, IGZO thin-film transistors (TFTs) have started to replace amorphous silicon TFTs for backplane drivers of flat-panel displays[1]. Flexible IGZO Schottky diodes operating beyond 2.45 GHz have already satisfied the principal frequency of smart phones[5]. Subthreshold Schottky-barrier IGZO TFTs have been demonstrated to be useful for sensor interface circuits in wearable electronics[6]. On the another hand, p-type oxide semiconductors are far behind mainly because of low on/off ratio, low hole mobility, and high subgap trap density[3]. However, p-type TFTs are essential in order to fabricate complementary integrated circuits with low static power consumption, high noise margin, high yield, and high reliability for actual applications. Realizing sophisticated all-oxide circuits operating in complementary mode has been challenging due to the difficulty in making high-performance p-type oxide TFTs matched with their n-type counterparts. Up to date, SnO is considered as the most promising p-type oxide due to its high field-effect hole mobility, good uniformity for large-scale fabrication, and high stability in ambient air [3,7]. To realize complementary inverters, one can either combine an n-type TFT and a p-type TFT or use two ambipolar TFTs. A rail-to-rail output voltage behavior can be easily achieved in the former but hard to achieve in latter case because neither of the two ambipolar TFTs can be fully switched off [8, 9, 10, 11]. The static current will also result in a static power consumption, which may be an issue in the case of large scale integration. Complementary inverters using n-type oxide (such as In_2O_3, SnO_2, IGZO, and ZnO) TFTs and p-type SnO TFTs have been reported[12-19]. Five-stage ring oscillators based on n-type ZnO and p-type SnO TFTs have been fabricated on glass and polyimide foil substrates[12, 13]. Common-source amplifiers, differential amplifiers, and logic gates have also been realized on paper substrates[20]. From the point of industrial application, high gain of complementary inverter is quite desirable in order to achieve large noise margins of the integrated circuits. However, to the best of our knowledge, the gains of the reported complementary inverters based on n- and p-type oxides are not higher than 30 under a supply voltage of 10 V until now [2, 3, 12, 13, 15, 16, 18, 24]. Furthermore, to date, the dynamic responses of oxide-based complementary logic gates with rail-to-rail output voltage behavior have not been reported yet. In this work, we fabricated

Manuscript received Nov. 12, 2017. This work was supported by the National Key Research and Development Program of China (Grant No. 2016YFA0301200 and 2016YFA0201800), the National Natural Science Foundation of China (Grant Nos. 11374185 and 11304180), Engineering and Physical Sciences Research Council (EPSRC) (Grant No. EP/N021258/1), China Postdoctoral Science Foundation funded project (2016M590634), the Key Research and Development Program of Shandong Province (2017GGX10111), the Natural Science Foundation of Jiangsu Province (BK20151255), Suzhou Planning Projects of Science and Technology (SYG201527 and SYG201616), and the Fundamental Research Fund of Shandong University (2016WLJH44).

Y. Li, J. Yang, Y. Wang, P. Ma, Y. Yuan, Z. Lin, L. Zhou, Q. Xin, and A. Song are with the Center of Nanoelectronics, State Key Laboratory of Crystal Materials, and School of Microelectronics, Shandong University, Jinan 250100, China (e-mail: xinq@sdu.edu.cn).

J. Zhang and A. Song are with the School of Electrical and Electronic Engineering, University of Manchester, Manchester M13 9PL, United Kingdom (e-mail: A.Song@manchester.ac.uk).

high-performance n-type IGZO TFTs and p-type SnO TFTs via room-temperature sputtering method which is suitable for large-scale fabrication and commercialization for transparent/flexible electronics. Moreover, we realized the integration of SnO and IGZO TFTs to achieve complementary inverters with extremely high voltage gain up to 112. Based on these inverters, we have realized 3-stage ring oscillators, NAND, and transmission gates with rail-to-rail output voltage behavior, and the dynamic responses of these logic gates are analyzed.

II. Experiments

The TFTs and circuits were fabricated on silicon substrate with 300-nm-thick thermally oxidized SiO_2. First, 50-nm-thick Al was deposited using thermal evaporation and patterned as gate electrode. Then, 30-nm-thick Al_2O_3 was deposited as dielectric by atomic-layer deposition (ALD) and patterned by wet etching. Next, 20-nm-thick SnO film was fabricated by radio-frequency magnetron sputtering and patterned by lift-off process followed by a post-annealing at 225 ºC for 1 h in air. After that, 24-nm-thick IGZO layer was deposited by sputtering method and patterned by lift-off process followed by the deposition of 50-nm-thick Ti as source/drain electrodes and interconnects using electron-beam evaporation. Finally, the TFTs and circuits were annealed at 100 ºC for 1 h in air. In this process, we set the geometric aspect ratio of inverters to be 5. The electrical characteristics were measured by source/measure unit (Agilent B2902A). The outputs of the logic gates and ring oscillators were measured by oscilloscope (Keysight MSOX6004A).

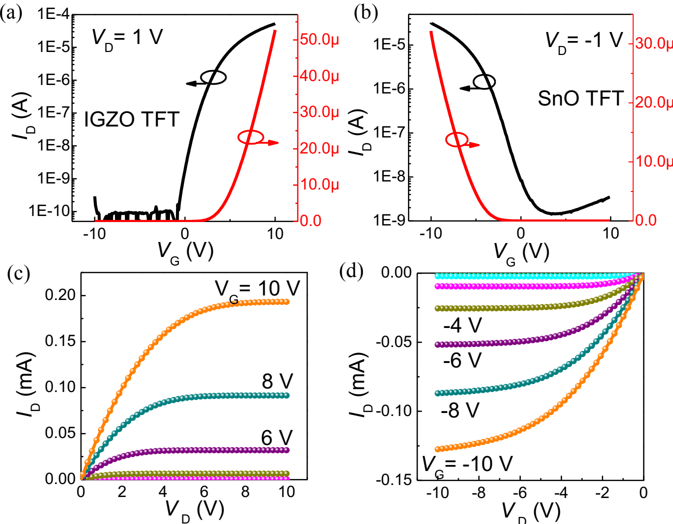

FIG. 1. Transfer characteristics of (a) the IGZO TFT and (b) the SnO TFT. Output characteristics of (c) the IGZO TFT and (d) the SnO TFT.

III. Results and Discussion

Figures 1(a) and (b) show the transfer characteristics of the IGZO TFT and the SnO TFT at drain voltage of 1 and -1 V, respectively. For the IGZO TFT, the mobility is 10.05 cm^2/V·s, the subthreshold swing, *SS*, is 0.86 V/dec, the on/off ratio is ~5.28×10^5, and the threshold voltage, V_{TH}, is 5.00 V. For the SnO TFT, the mobility is 1.19 cm^2/V·s, V_{TH} is -5.05 V, *SS* is 1.50 V/dec, and the on/off ratio is 2.2×10^4 which is among the highest values of the reported SnO TFTs[3, 21-22]. The output curves of the IGZO TFT and the SnO TFT are shown in Figs. 1(c) and (d), respectively, indicating ideal saturation characteristics and ohmic contacts between the source/drain electrodes and the active layers. The comparable performance of SnO TFT and IGZO TFT guarantees the high-performance complementary inverter based on SnO TFT and IGZO TFT.

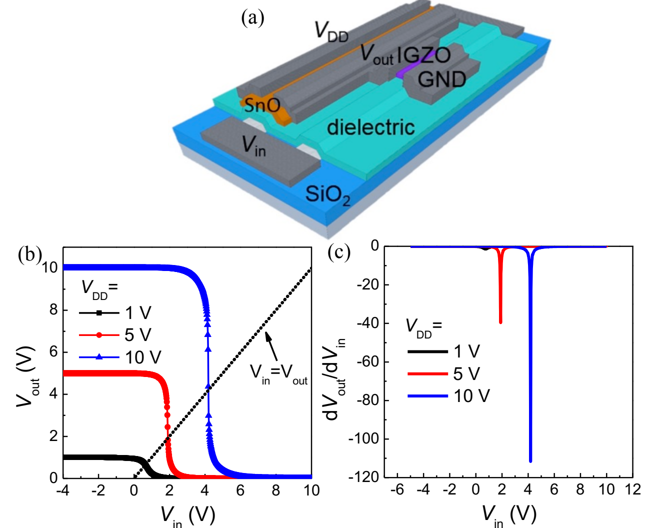

FIG. 2. (a) Schematic diagram of a complementary inverter based on a p-type SnO TFT and an n-type IGZO TFT. (b) Output voltages (V_{out}) and (c) gains of the complementary inverter as a function of input voltages (V_{in}) at different supply voltages (V_{DD}).

Figure 2(a) shows the schematic diagram of a complementary inverter based on a p-type SnO TFT and an n-type IGZO TFT. The operations of the IGZO/SnO complementary inverter at different supply voltages, V_{DD}, are shown in Fig. 2(b). The voltage gain at V_{DD} = 10 V reaches as high as 112 (Fig. 2(c)), which is the highest value among complementary inverters using n- and p-type oxide TFTs below 10 V supply voltage [2, 3, 12, 13, 15, 16, 18, 24]. The threshold voltage of the inverter, where V_{in} = V_{out}, is found to be 1.97 V and 4.25 V at V_{DD} = 5 V and 10 V, respectively. They are close to the ideal value, V_{DD}/2. The threshold voltage of the inverter can be further optimized by increasing the geometric aspect ratio, which is defined as the ratio of $(W/L)_p$ to $(W/L)_n$, where $(W/L)_p$ and $(W/L)_n$ are the width-to-length ratio of SnO channel and IGZO channel, separately. The input-low voltage (V_{IL}) and the input-high voltage (V_{IH}) are defined as the point where $d(V_{out})/d(V_{in})$ = -1. When V_{DD} = 5 V, V_{IL} = 1.52 V and V_{IH} = 2.26 V. When V_{DD} = 10 V, V_{IL} = 3.54 V and V_{IH} = 4.78 V. The transition region can be determined by (V_{IH} − V_{IL}) which equals 0.74 V and 1.24 V at V_{DD} = 5 V and 10 V, respectively. When V_{DD} = 5 V, the noise margin high is 2.74 V by using (V_{DD} − V_{IH}), and the noise margin low is 1.52 V which equals V_{IL}. When V_{DD} = 10 V, the noise margin high is 5.22 V and the noise margin low is 3.54 V. The large values indicate that the inverter could withstand a high noise level. The high gain and large noise

margin of inverters ensure that the logic gates and complex circuits for actual applications based on these inverters can be realized and work reliably.

Figure 3(a) shows the schematic diagram of complementary inverter based on a p-type SnO TFT and an n-type IGZO TFT. In the Fig. 3(b), we can see, input pulse, V_{in}, and the corresponding output, V_{out}, at 4-kHz operating frequency. The delay time of the inverter is found to be 27.75 µs. Figures 3(c) and (d) illustrate the schematic diagram and performance of a two-input NAND gate based on two complementary inverters, respectively. The output of the NAND is '0' only when both of the inputs are set to '1'. Figures 3(e) and (f) show the schematic diagram and performance of a transmission gate, respectively. The output signal, *B*, equals to input signal, *A*, only when the control signal, *C*, is '1'. When *C* is set to '0', *B* is always '0'.

All of the logic gates demonstrate rail-to-rail voltage swing from 0 to 10 V at V_{DD} = 10 V. This can be attributed to the robust complementary mode of operation of the IGZO/SnO inverter.

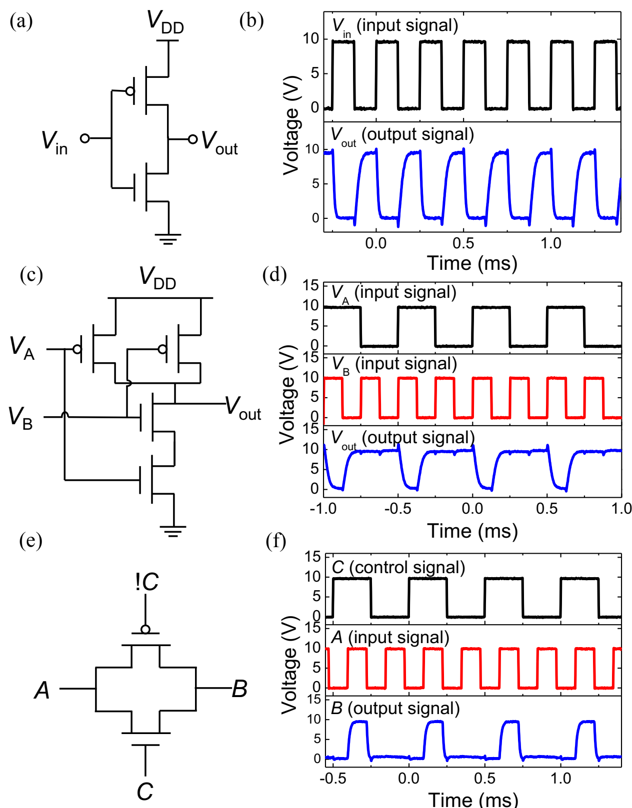

FIG. 3. (a) Schematic diagram and (b) output characteristics of the complementary inverter based on a p-type SnO TFT and an n-type IGZO TFT. (c) Schematic diagram and (d) output characteristics of the SnO/IGZO NAND gate. (e) Schematic diagram and (f) output characteristics of the SnO/IGZO transmission gate.

Figures 4(a) and (b) show the layout and the schematic diagram of the 3-stage ring oscillator with an output buffer, respectively. Figure 4(c) describes the operation of the ring oscillator at different V_{DD}. The oscillation frequency of the ring oscillator increases with increasing of V_{DD}. When V_{DD} = 20 V, the oscillator frequency reaches 32.87 kHz. The stage delay of the 3-stage ring oscillator can be calculated with ($1/6f$), where f is the oscillation frequency. The stage delay is found to be 5.07 µs when V_{DD} = 20 V. Such stage delay is in the same order of magnitude compared to the 5-stage ring oscillator based on ZnO and SnO TFTs[12, 13].

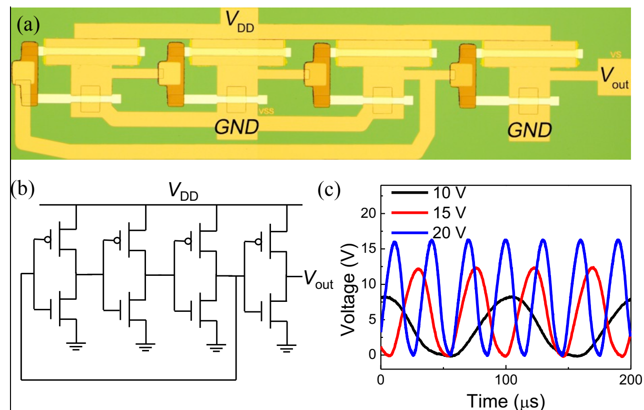

FIG. 4. (a) Layout of the 3-stage ring oscillator with an output buffer. (b) Schematic diagram of a 3-stage ring oscillator with an output buffer. (c) Output voltages of the complementary ring oscillator as a function of time at different V_{DD}.

IV. Conclusions

In this letter, complementary inverters with extremely high voltage gain up to 112 at V_{DD} = 10 V are fabricated based on the n-type IGZO and the p-type SnO TFTs. The dynamic responses of the inverter, NAND and transmission gates are analyzed. The delay time of the inverter is 27.75 µs at V_{DD} = 10 V. All of the fabricated logic gates show ideal rail-to-rail output voltage behavior. The output frequency of 3-stage ring oscillator reaches 32.87 kHz when V_{DD} = 20 V. Our study indicates that other complementary logic gates and sophisticated circuits for potential larger-area transparent/flexible electronics with large noise margin and low static power consumption can be realized based on n-type IGZO and p-type SnO TFTs.

References

[1] T. Kamiya, K. Nomura, and H. Hosono, "Present status of amorphous In-Ga-Zn-O thin-film transistors," *Sci. Technol. Adv. Mater.,* vol. 11, no. 4, p. 044305, Sep. 2010, doi: 10.1088/1468-6996/11/4/044305.

[2] E. Fortunato, P. Barquinha, and R. Martins, "Oxide semiconductor thin-film transistors: a review of recent advances," *Adv. Mater.,* vol. 24, no. 22, pp. 2945-2986, Jun. 2012, doi: 10.1002/adma.201103228.

[3] Z. Wang, P. K. Nayak, J. A. Caraveo-Frescas, and H. N. Alshareef, "Recent Developments in p-Type Oxide Semiconductor Materials and Devices," *Adv Mater,* vol. 28, no. 20, pp. 3831-3892, May 2016, doi: 10.1002/adma.201503080.

[4] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature,* vol. 432, no. 7016, pp. 488-492, Nov. 2004, doi: 10.1038/nature03090.

[5] J. Zhang, Y. Li, B. Zhang, H. Wang, Q. Xin, and A. Song, "Flexible indium-gallium-zinc-oxide Schottky diode operating beyond 2.45 GHz," *Nat. Commun.,* vol. 6, p. 7561, Jul. 2015, doi: 10.1038/ncomms8561.

[6] S. Lee, and A. Nathan, "Subthreshold Schottky-barrier thin-film transistors with ultralow power and high intrinsic gain," *Science,* vol. 354, no. 6310, pp. 302-304, Oct. 2016, doi: 10.1126/science.aah5035.

[7] Y. Ogo, H. Hiramatsu, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, "p-channel thin-film transistor using p-type oxide

semiconductor, SnO," *Appl. Phys. Lett.,* vol. 93, no. 3, p. 032113, Jul. 2008, doi: 10.1063/1.2964197.

[8] K. Nomura, T. Kamiya, and H. Hosono, "Ambipolar Oxide Thin-Film Transistor," *Adv. Mater.*, vol. 23, no. 30, pp. 3431-3234, Aug. 2011, doi: 10.1002/adma.201101410.

[9] L. Y. Liang, H. T. Cao, X. B. Chen, Z. M. Liu, Z. Fei, H. Luo, J. Li, Y. C. Lu, and W. Lu, "Ambipolar inverters using SnO thin-film transistors with balanced electron and hole mobilities," *Appl. Phys. Lett.,* vol. 100, no. 26, p. 263502, Jun. 25, 2012, doi: 10.1063/1.4731271.

[10] H. Luo, L. Liang, H. Cao, M. Dai, Y. Lu, and M. Wang, "Control of Ambipolar Transport in SnO Thin-Film Transistors by Back-Channel Surface Passivation for High Performance Complementary-like Inverters," *ACS Appl. Mater. Interfaces,* vol. 7, no. 31, pp. 17023-17031, Aug. 12, 2015, doi: 10.1021/acsami.5b02964.

[11] P.-T. Liu, Y.-T. Chou, L.-F. Teng, and C.-S. Fuh, "High-gain complementary inverter with InGaZnO/pentacene hybrid ambipolar thin film transistors," *Appl. Phys. Lett.,* vol. 97, no. 8, p. 083505, 2010, doi: 10.1063/1.3483616.

[12] I.-C. Chiu, Y.-S. Li, M.-S. Tu, and I.-C. Cheng, "Complementary Oxide-Semiconductor-Based Circuits With n-Channel ZnO and p-Channel SnO Thin-Film Transistors," *IEEE Electron Device Lett.,* vol. 35, no. 12, pp. 1263-1265, Dec. 2014, doi: 10.1109/led.2014.2364578.

[13] Y.-S. Li, J.-C. He, S.-M. Hsu, C.-C. Lee, D.-Y. Su, F.-Y. Tsai, and I.-C. Cheng, "Flexible Complementary Oxide-Semiconductor-Based Circuits Employing n-Channel ZnO and p-Channel SnO Thin-Film Transistors," *IEEE Electron Device Lett.,* vol. 37, no. 1, pp. 46-49, Jan. 2016, doi: 10.1109/led.2015.2501843.

[14] R. Martins, A. Nathan, R. Barros, L. Pereira, P. Barquinha, N. Correia, R. Costa, A. Ahnood, I. Ferreira, and E. Fortunato, "Complementary metal oxide semiconductor technology with and on paper," *Adv. Mater.,* vol. 23, no. 39, pp. 4491-4496, Oct. 2011, doi: 10.1002/adma.201102232.

[15] P. K. Nayak, J. A. Caraveo-Frescas, Z. Wang, M. N. Hedhili, Q. X. Wang, and H. N. Alshareef, "Thin Film Complementary Metal Oxide Semiconductor (CMOS) Device Using a Single-Step Deposition of the Channel Layer," *Sci. Rep.,* vol. 4, p. 4672, Apr. 2014, doi: 10.1038/srep04672.

[16] H. Yabuta, N. Kaji, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, "Sputtering formation of p-type SnO thin-film transistors on glass toward oxide complimentary circuits," *Appl. Phys. Lett.,* vol. 97, no. 7, p. 072111, Aug. 2010, doi: 10.1063/1.3478213.

[17] Z. Wang, H. A. Al-Jawhari, P. K. Nayak, J. A. Caraveo-Frescas, N. Wei, M. N. Hedhili, and H. N. Alshareef, "Low temperature processed complementary metal oxide semiconductor (CMOS) device by oxidation effect from capping layer," *Sci. Rep.,* vol. 5, p. 9617, Apr. 2015, doi: 10.1038/srep09617.

[18] J. Zhang, J. Yang, Y. Li, J. Wilson, X. Ma, Q. Xin, and A. Song, "High Performance Complementary Circuits Based on p-SnO and n-IGZO Thin-Film Transistors," *Materials,* vol. 10, no. 3, p. 319, Mar. 2017, doi: 10.3390/ma10030319.

[19] Dhananjay, C.-W. Chu, C.-W. Ou, M.-C. Wu, Z.-Y. Ho, K.-C. Ho, and S.-W. Lee, "Complementary inverter circuits based on p-SnO_2 and n-In_2O_3 thin film transistors," *Appl. Phys. Lett.,* vol. 92, no. 23, p. 232103, Jun. 2008, doi: 10.1063/1.2936275.

[20] R. F. P. Martins, A. Ahnood, N. Correia, L. M. N. P. Pereira, R. Barros, P. M. C. B. Barquinha, R. Costa, I. M. M. Ferreira, A. Nathan, and E. M. C. Fortunato, "Recyclable, Flexible, Low-Power Oxide Electronics," *Adv. Funct. Mater.,* vol. 23, no. 17, pp. 2153-2161, May 2013, doi: 10.1002/adfm.201202907.

[21] H.-J. Kim, C.-Y. Jeong, S.-D. Bae, J.-H. Lee, and H.-I. Kwon, "Charge Transport Mechanism in p-Channel Tin Monoxide Thin-Film Transistors," *IEEE Electron Device Lett.,* vol. 38, no. 4, pp. 473-476, Apr. 2017, doi: 10.1109/led.2017.2672730.

[22] P.-C. Chen, Y.-C. Chiu, G.-L. Liou, Z.-W. Zheng, C.-H. Cheng, and Y.-H. Wu, "Performance Enhancements in p-Type Al-Doped Tin-Oxide Thin Film Transistors by Using Fluorine Plasma Treatment," *IEEE Electron Device Lett.,* vol. 38, no. 2, pp. 210-212, Feb. 2017, doi: 10.1109/led.2016.2646378.

[23] P. -C. Chen, Y.-C. Chiu, Z.-W. Zheng, M.-H. Lin, C.-H. Cheng, G.-L. Liou, H.-H. Hsu, and H.-L. Kao, "Fast Low-Temperature Plasma Process for the Application of Flexible Tin-Oxide-Channel Thin Film Transistors," *IEEE Trans. Nanotechnol.,* vol. 16, no. 5, pp. 876-879, Sep. 2017, doi: 10.1109/tnano.2017.2719946.

[24] A. Dindar, J. B. Kim, C. Fuentes-Hernandez, and B. Kippelen, "Metal-oxide complementary inverters with a vertical geometry fabricated on flexible substrates," *Appl. Phys. Lett.,* vol. 99, p. 172104, Oct. 2011, doi: 10.1063/1.3656974.