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# Energy Efficiency of Low Swing Signaling for Emerging Interposer Technologies

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## ABSTRACT

Interconnects often constitute the major bottleneck in the design process of low power integrated circuits (IC). Although 2.5-D integration technologies support physical proximity, the dissipated power in the communication links remains high. In this work, the additional power savings for interposer-based interconnects enabled by low swing signaling is investigated. The energy consumed by a low swing scheme is, therefore, compared with a full swing solution and the critical length of the interconnect, above which the low swing solution starts to pay off, is determined for diverse interposer technologies. The energy consumption is compared for three different substrate materials, silicon, glass, and organic. Results indicate that the higher the load capacitance of the communication medium is, the greater the energy savings of the low swing circuit are. Specifically, in cases that electrostatic discharge (ESD) protection is required, the low swing circuit is always superior in terms of energy consumption due to the high capacitive load of the ESD circuit, regardless the substrate material and the link length. Without ESD protection, the highest critical length is about 380  $\mu\text{m}$  for glass and organic interposers. To further explore the limits of power reduction from low swing signaling for 2.5-D ICs, the effect of typical interconnect parameters such as width and space on the energy efficiency of low swing communication is evaluated.

## CCS CONCEPTS

• **Hardware**  $\rightarrow$  **3D integrated circuits; Metallic interconnect; Interconnect power issues;**

## KEYWORDS

Interconnect, Low Swing, Interposer, 2.5-D Integration, Energy Efficiency

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## 1 INTRODUCTION

In the deep-submicrometer era, the demand for higher energy efficiency grows. Meeting power requirements becomes increasingly difficult, since the energy required for transferring data does not scale at the same pace as technology, due to the non-decreasing system size [1]. In [2], the power dissipated in wires is shown to constitute up to 40% of the total on-chip power, whilst driving the off-chip interconnects can consume 65% of the total power. Although the scaling of technology has led to the reduction of energy consumption of digital logic circuits, the increasing wire density in combination with the non-decreasing link length has a negative effect on the power dissipation of the interconnects. Future systems with processor performance in the order of 3 Tera-operands/sec, are predicted to consume up to 58 W for transferring data, assuming 1 mm interconnect length on average [3].

To decrease the interconnect length and achieve higher integration density, interposer technologies, or 2.5-D integration, have emerged as a promising solution [4]. This integration paradigm allows multiple dies to be integrated on both sides of the interposer and be connected through redistribution layers (RDL), allowing an interconnect pitch comparable to on-chip wires and several times smaller than Printed Circuit Board (PCB) traces. As silicon-based 2.5-D ICs have been commercialised [5], different materials for interposer substrates are developed, moving from standard silicon [6] to other alternatives, such as glass [7] and organic substrate [8],[9]. Although these materials exhibit lower conductivity and thus provide better insulation, the problem of high interconnect power remains crucial, due to additional load capacitance from Through Package Via (TPV) and bump bonding. In other words, the physical proximity of the components enabled by 2.5-D integration offers limited gain in power.

A drastic way to accomplish remarkable energy drop is the use of low swing signaling [10]. Several works have proposed different low swing techniques, where the supported communication includes chip-to-chip interconnects at the package or PCB level ([11]–[14]). Consequently, the potential improvement in the energy efficiency of inter-chip communication for interposers has yet to be determined. In this paper, the benefits of utilising low swing for inter-chip communication in 2.5-D integration are quantified.

The power benefits due to the shorter physical distance between components in 2.5-D systems utilising full swing interconnects have been demonstrated in [15], [16]. The circuits used to drive the interconnect in the prior art are not well-suited for low swing communication. Consequently, to investigate the effectiveness of the low swing paradigm in different interposer technologies, an appropriate single-ended transceiver proposed in [17] is employed.

This circuit supports off-chip communication in interposers and offers ultra low level of voltage swing. This transceiver exhibits a 4× decrease in power over full swing communication as shown in [17] for a specific, however, link length. Therefore, this circuit is used as the baseline transceiver to investigate the potential of low swing communication in several physical media developed for 2.5-D integrated systems.

The energy efficiency of the low swing transceiver is accurately determined and the primary power consuming factors are highlighted for three different substrate materials, silicon, glass, and organic. Additionally, the critical length above which the application of the low swing scheme starts to offer energy savings in comparison with the full swing is determined for each substrate material. Finally, the effect of wire density on the energy efficiency of the low swing circuit is ascertained. In this way, useful rules of thumb are provided regarding the use of low swing communication mechanisms for 2.5-D integrated systems.

The paper is structured as follows. In Section 2, the characteristics of different technologies along with electrical models are presented. The utilised low swing transceiver is discussed in Section 3. The energy efficiency for different technologies, interconnect lengths and wire densities is investigated in Section 4 and conclusions are drawn in Section 5.

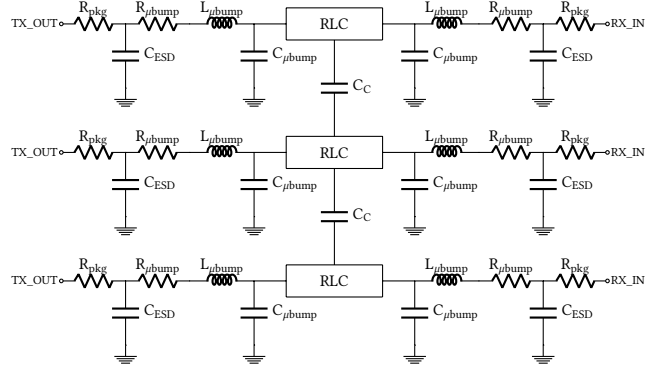
## 2 INTERCONNECT MODELING

The models for different types of interconnects and the electrical characteristics of each type of interconnect are described in this section. The investigated interconnect technologies and the related RDL parameters of each technology are listed in Table 1. Three types of interposers are considered. For the silicon interposer, the top metal layers are utilised, thus the physical parameters of global wires are used according to [18]. However, since the RDL on top of interposers is usually larger, a second case with more realistic wire models is also considered [6], where SiO<sub>2</sub> is used as dielectric with relative dielectric permittivity  $\epsilon_r = 3.9$ . The parameters of the interconnects on a glass and organic interposer are derived from [7] and [8], respectively. An Ajinomoto Build-up Film (ABF) is used for the insulation of metal layers on the glass interposer, with  $\epsilon_r = 3.35$ . In the remaining cases where the dielectric material is not specified, polyimide is assumed for the sake of simplicity, with  $\epsilon_r = 3.5$ .

**Table 1: Interconnect parameters including the minimum width ( $W$ ), space ( $S$ ), and thickness ( $T_W$ ) of the wires, the interlayer dielectric thickness ( $T_D$ ) and dielectric constant of the passivation layer.**

Interposer Technology	$W$ [ $\mu\text{m}$ ]	$S$ [ $\mu\text{m}$ ]	$T_W$ [ $\mu\text{m}$ ]	$T_D$ [ $\mu\text{m}$ ]	$\epsilon_r$
Silicon [18]	0.45	0.45	1.2	0.2	3.5
Silicon [6]	2	2	3	1.5	3.9
Glass [7]	3	3	4	7	3.35
Organic [8]	3	3	2.5	2.5	3.5

The equivalent circuit of an interposer interconnect consisting of three adjacent lines is illustrated in Fig. 1. In this model, in addition to the wire electrical parameters, electrostatic discharge (ESD) protection, as well as the microbump impedance characteristics are included according to [19]. Furthermore, the RLC elements of microbumps, reported in Table 2, are assumed equal for all of the interposer materials.

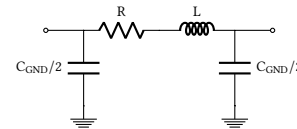


**Figure 1: Electrical model of three interconnect lines for an interposer technology.**

**Table 2: RLC elements of microbumps and package.**

$R_{pkg}$ [ $\Omega$ ]	$R_{bump}$ [ $\Omega$ ]	$L_{bump}$ [nH]	$C_{bump}$ [fF]
0.014	0.095	0.053	5.4

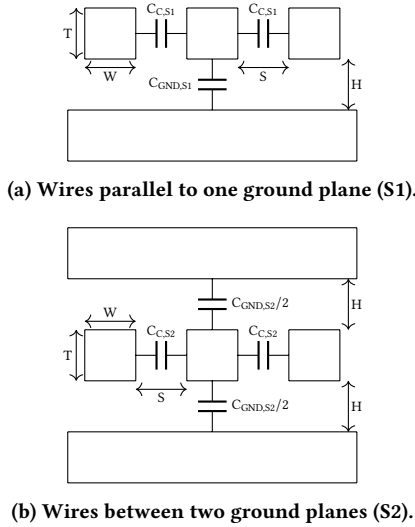
The wires are modeled as distributed interconnects with multiple  $\pi$ -type segments as depicted in Fig. 2. The resistance and wire inductance are estimated according to [18] and the mutual inductance is not accounted for as its effect is negligible [15], while expressions from [20] are utilised for the wire capacitance. Two primary structures are utilised for modeling the capacitance of the interconnects. In the first geometry (S1), the wires are adjacent to a ground plane (Fig. 3a), while the second structure (S2) consists of wires sandwiched in-between two ground planes (Fig. 3b).



**Figure 2: A  $\pi$ -type segment.**

To calculate the wire capacitances, each interconnect geometry is matched to one of the two structures. Specifically, in case of the 2 + 0 + 2 glass interposer stack-up of [7], the glass core is 100  $\mu\text{m}$  thick and, therefore, is safely assumed to behave as an insulator, as the glass resistivity is very high, from  $1 \times 10^{12}$  to  $1 \times 10^{16}$   $\Omega\text{-cm}$  [21]. Hence, the capacitances of the bottom wires follow the closed-form expressions for S1, where only one ground plane is considered. The organic interposer of [8], is modeled in the exact same way

as glass, due to the low permittivity ( $\epsilon_r = 4.4$  [22]) of the organic materials. Alternatively, the silicon substrate, with  $\epsilon_r = 11.2$  [22], is electrically modeled by a ground plane. Thus, the capacitances of the silicon interposer with wire parameters described in [18] are evaluated by utilising the expressions for the second structure (S2). The estimated electrical characteristics of the wires per unit length for each technology are reported in Table 3. The total capacitance is calculated as  $C_{total} = C_{GND} + 2C_C$  for each of the two structures S1 and S2.



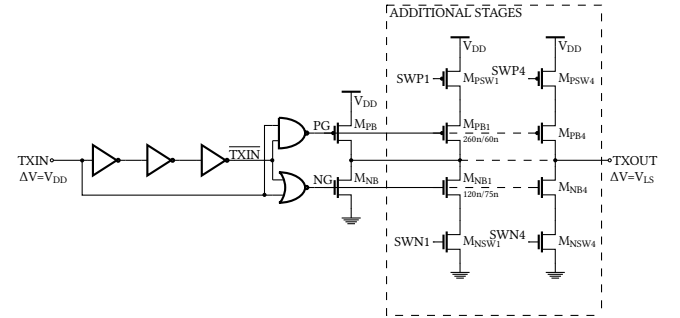
**Figure 3: Cross-sectional view of typical interconnect structures, where (a) one ground plane is present and (b) interconnects are flanked by two ground planes.**

### 3 LOW SWING TRANSCEIVER

A brief description of the low swing transceiver of [17] is provided in this section. This circuit consists of a dynamic low swing tunable transmitter (DLST-TX) and an inverter-based tunable receiver (INVT-RX). The schematic diagram of the transmitter is depicted in Fig. 4. The conversion of signal from full to low swing is achieved through a short propagation delay, introduced by a delay line (three inverters connected in series), during which the output of one of the transistors  $M_{NB}$  or  $M_{PB}$  is turned on, while in steady mode (i.e. the input TXIN does not switch) both are turned off. This short delay time is not sufficient for the output buffer to fully charge or discharge the load capacitance, hence, the voltage range decreases. Consequently, the voltage varies by  $\pm\Delta V$  around a constant  $V_{DC}$ , which is selected equal to  $V_{DD}/2$ . To restore voltage swing, the receiver incorporates a CMOS inverter used as a front end amplifier.

In [17], the additional stages illustrated in Fig. 4 are used for trimming the driving strength of the transceiver in order to compensate process variability. However, in this work, the transistors added in parallel to  $M_{NB}$  and  $M_{PB}$  are rather used to adjust the level of the low voltage swing  $V_{LS}$ , since  $V_{LS}$  depends on the load capacitance, which, in turn, also depends on the interposer technology.  $V_{LS}$  is regulated by the number of the activated transistors  $M_{PB1}$  to

$M_{PB4}$  and  $M_{NB1}$  to  $M_{NB4}$  through the respective switches  $M_{PSW1}$  to  $M_{PSW4}$  and  $M_{NSW1}$  to  $M_{NSW4}$ . Note that the driving strength of each stage is double than the previous stage.

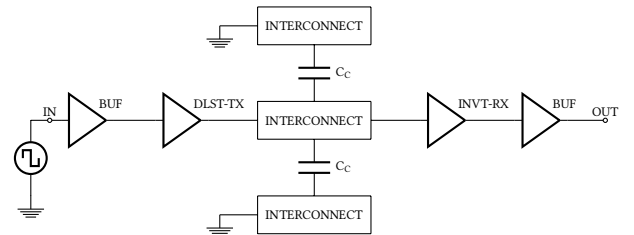


**Figure 4: Transmitter schematic diagram.**

### 4 RESULTS AND DISCUSSION

The results relating to the energy efficiency of the low swing transceiver for the investigated communication channels are presented in this section. In Subsection 4.1, for each interposer technology the energy per bit of the low swing (LS) interconnect is compared with that of the full swing (FS) with and without ESD capacitance. A minimum voltage swing of  $V_{LS} = 100$  mV and minimum wire pitch are considered in this scenario. The technology that can benefit more from the implementation of low swing signaling is determined. Furthermore, the length at which the two schemes have equal energy consumption is evaluated. In Subsection 4.2, the energy efficiency of the low swing versus the full swing transceiver is explored for varying wire densities by adjusting the width and space of the wires.

The transceiver test circuit, designed in a 65 nm technology with 1.2 V supply voltage ( $V_{DD}$ ), is illustrated in Fig. 5. The test circuit consists of three parallel wires; the middle wire is connected to a signal generator that operates at 1 Gb/s speed with 20 ps transition times, while the two neighbouring wires are connected to ground. The energy per bit of both full and low swing transceivers is evaluated for a pseudo-random 200 bit long sequence in nominal conditions (typical device corners, 27°C). The two buffers (noted as BUF) preceding the transmitter and following the receiver are used to, respectively, model the driving strength and load of the core logic circuits connected by the transceiver.



**Figure 5: Transceiver test circuit.**

Note that the energy results do not critically depend on the choice of the LS circuit, but primarily on the level of voltage swing

**Table 3: Electrical characteristics of wires for minimum pitch.**

Interconnect technology	Structure	$R$ [ $\Omega/\text{mm}$ ]	$L$ [ $\text{nH}/\text{mm}$ ]	$C_{GND}$ [ $\text{fF}/\text{mm}$ ]	$C_C$ [ $\text{fF}/\text{mm}$ ]	$C_{total}$ [ $\text{fF}/\text{mm}$ ]
Silicon interposer [18]	2	40.74	1.52	222.55	52.45	327.45
Silicon interposer [6]	1	3.67	1.29	85.49	73.49	232.47
Glass interposer [7]	1	1.83	1.23	24.09	69.16	162.41
Organic interposer [8]	1	2.93	1.28	68.79	46.09	160.97

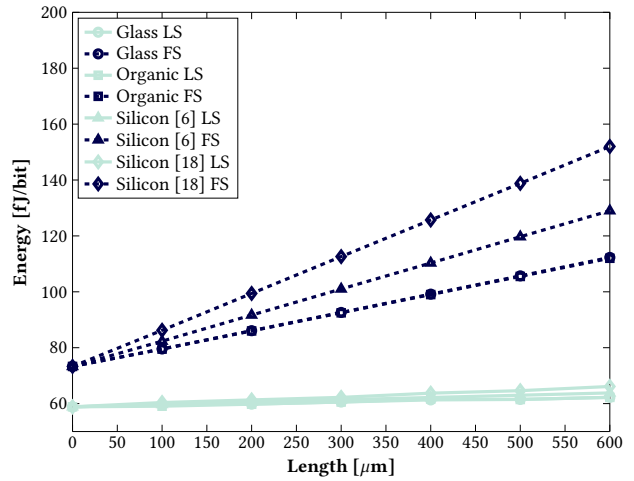
and the characteristics of the communication medium. A different implementation of the LS transceiver would only affect the overhead in power, introduced by the transmitter and receiver circuits, required to reduce and restore the voltage level. Therefore, the energy of the low swing scheme would be shifted based on the efficiency of the implementation, however, the behaviour of the energy would remain the same.

### 4.1 Critical length for minimum wire pitch

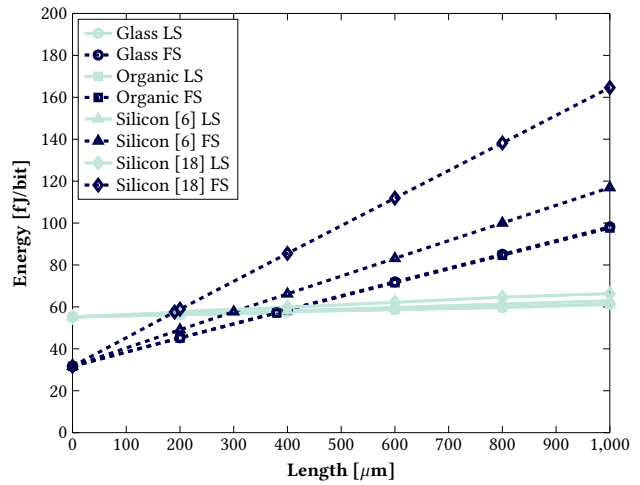
The simulated energy efficiency versus the interconnect length for each interposer technology is plotted in Fig. 6. The low swing voltage is kept constant at 100 mV and the interconnect length ranges from 10  $\mu\text{m}$  up to 1 mm. The low boundary of the explored range corresponds to the case where the link is so short that the wire parasitics are negligible. As shown, the energy per bit increases linearly with the increase in length for all different technologies. This behaviour is expected since the power dissipation is proportional to capacitance and longer length corresponds to higher load capacitance. In addition, the slope of the energy depends primarily on the level of voltage swing and secondarily, on the wire capacitance of each technology. Therefore, the energy consumed by the low swing scheme remains relatively steady for each technology. On the contrary, the energy of the full swing scheme increases at a higher pace and the interconnect technology with the steepest slope (i.e. the greatest increase in energy) is the silicon interposer with wire parameters described in [18], which has the highest total wire capacitance.

In Fig. 6a, where the ESD capacitance is equal to 50 fF based on [16],[19], the low swing transceiver for all of the interposer technologies features always higher energy efficiency than the full swing regardless the link length. This behaviour highlights the limited benefit of interposer technologies to reduce the power dissipation of interconnects and the capability of low swing signaling to effectively enhance energy efficiency. The energy gains are even higher for longer interconnects. At 500  $\mu\text{m}$  length the ratio of the energy of the full swing to the low swing scheme is 2.15, while at 1 mm length is estimated 2.9.

Removing the ESD capacitance leads to a considerable reduction of energy for the full swing transceiver, as illustrated in Fig. 6b, whereas the shift of the low swing is hardly noticeable. For short interconnect lengths, the energy per bit of the low swing solution exceeds that of the full swing. This behaviour indicates that the power overhead of the low swing circuit, which is dominantly generated by the transmitter to decrease the voltage level, is higher than the power dissipation of full swing within this length range.



(a) With ESD protection.



(b) Without ESD protection.

**Figure 6: Energy vs interconnect length for different interposer technologies, where (a) the ESD capacitance is  $C_{ESD} = 50$  fF and (b) the  $C_{ESD}$  is not considered.**

Hence, this case indicates that the low swing scheme is not suitable for technologies that can support high physical proximity of components, such as in [16].

The critical length along with the total wire capacitance per mm for each interconnect technology are listed in Table 4. As shown, the critical length and the  $C_{total}$  are strongly correlated. The higher

the  $C_{total}$  is, the shorter the critical length. Results show that the critical length is the shortest for the silicon interposer technology with the lowest pitch described in [18] and the longest for the glass and organic interposers, demonstrating that for silicon substrates the application of low swing signaling is more beneficial.

## 4.2 Exploration of energy efficiency for different wire densities

To provide the boundaries of energy gains of low swing signaling in the case of relaxed area constraints, an exploration of the energy efficiency with respect to wire parameters, such as width and space, is conducted. The energy efficiency is estimated as the ratio of the energy per bit of the full swing to that of the low swing solution (denoted as  $E_{FS}/E_{LS}$ ). The  $V_{LS}$  is kept constant at 100 mV as well as the length at 300  $\mu\text{m}$ , while ESD protection is excluded. The upper limits of width and space are considered 10 $\times$  and 5 $\times$ , respectively, larger than the minimum corresponding value supported by each technology for the glass, organic and the silicon interposer described in [6], while for the silicon interposer in [18] are 5 $\times$  and 2.5 $\times$ , respectively.

Results demonstrate that the highest energy gains in absolute power terms are exhibited by the interconnects of silicon interposers, as shown in Figures 7 and 8. The highest ratio  $E_{FS}/E_{LS}$  is demonstrated for maximum width and minimum space, which is 2.1 and 1.8 for the interconnect in [18] and [6], respectively. In this case, the power dissipation of the full swing scheme is high since both  $C_{GND}$  and  $C_C$  are significant, resulting in a high capacitive load. On the contrary, the application of low swing signaling is less beneficial for low width and large space, where the energy consumption of the full swing decreases. Especially, the efficiency of the interconnect in [6] drops below 1 in this area, which means that the energy consumption of the low swing is higher than the full swing circuit. Furthermore, the energy for both types of interconnects shows a strong dependence on the width of the wires, while the effect of space is rather weak, diminishing fast farther from the minimum value.

Interconnects on glass and organic interposers feature lower energy efficiency by the implementation of the low swing scheme, as illustrated in Figures 9 and 10.  $E_{FS}/E_{LS}$  follows the same trend for the organic interposer as for the silicon interposers, which means that the width of wires has the highest impact on power and thus, on the energy efficiency.  $E_{FS}/E_{LS}$  reaches the highest value of 1.5 for maximum width and decreases at about 0.9 for minimum width. Alternatively, the power dissipation for the glass interposer is highly affected by the spacing of wires. Due to the large thickness of the passivation layer of the glass interposer, the largest component of the  $C_{total}$  is due to the coupling of the wires. Consequently, larger spacing results in the drop of the power dissipated in the link and diminishes the efficiency of low swing. The glass interposer benefits less by the low swing scheme.  $E_{FS}/E_{LS}$  ranges from 0.8 for maximum space and low width to 1.15 for minimum space and maximum width.

## 5 CONCLUSION

In this work, the increase in energy efficiency of interposer-based interconnects through low swing signaling is investigated. Results

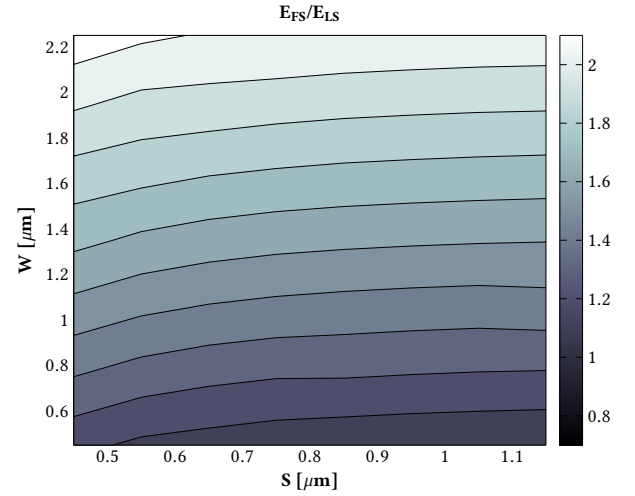


Figure 7: Energy efficiency for the silicon interposer with wire parameters described in [18].

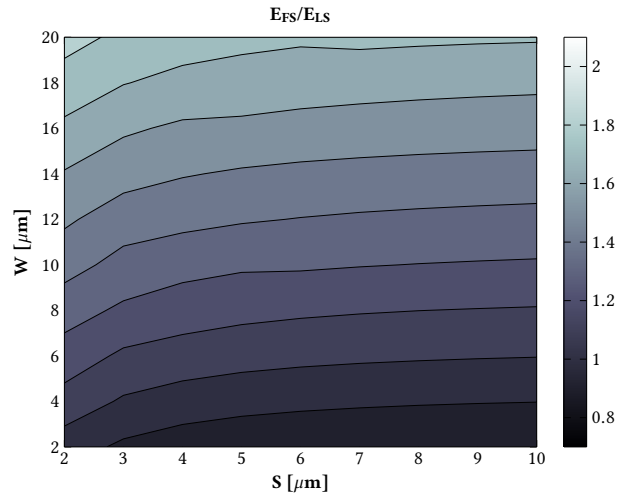
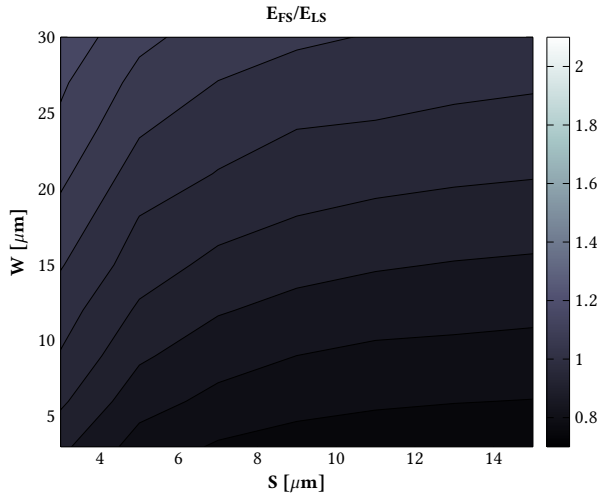
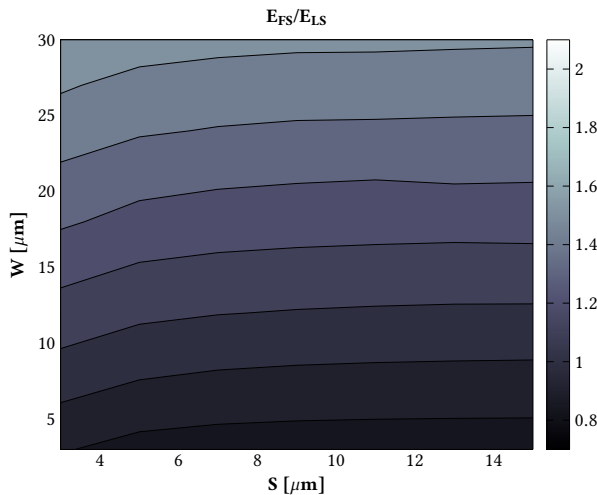


Figure 8: Energy efficiency for the silicon interposer described in [6].

imply that energy consumption depends highly on the total capacitance of the driven load and not just the interconnect length. This behaviour shows that only the physical proximity enabled by the interposers may not be sufficient to provide the energy efficiency required by future interconnects. Low swing techniques can decrease the power dissipation of inter-chip communication for 2.5-D integrated systems. The low swing solution provides higher power savings for silicon interposers which have the highest wire capacitance. Furthermore, when ESD protection is required, the low swing signaling is always superior to the full swing. Without  $C_{ESD}$ , for short interconnect lengths, the power overhead of the low swing circuit is higher than the power dissipation of the full swing. In this case, the critical length at which the two circuits demonstrate equal energy consumption is the shortest for silicon interposers

**Table 4: Critical length for different interposer technologies.**

Interconnect technology	Silicon interposer [18]	Silicon interposer [6]	Glass interposer [7]	Organic interposer [8]
Critical length [ $\mu\text{m}$ ]	190	300	380	380
$C_{total}$ [fF/mm]	327.45	232.47	162.41	160.97

**Figure 9: Energy efficiency for the glass interposer.****Figure 10: Energy efficiency for the organic interposer.**

and reaches up to 380  $\mu\text{m}$  for glass and organic interposers. Finally, the potential decrease in energy with respect to the wire density is investigated. The energy efficiency of the low swing signaling increases in the case where large wire width in combination with low spacing are required.

## ACKNOWLEDGMENTS

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