GaN metal-oxide-semiconductor high-electron-mobility transistors using thermally evaporated SiO as the gate dielectric

DOI:
10.1088/1361-6641/aad8d7

Document Version
Accepted author manuscript

GaN metal-oxide-semiconductor high-electron-mobility transistors using thermally evaporated SiO as the gate dielectric

Gengchang Zhu,[1] Yiming Wang,[1] Qian Xin,[1,2] Mingsheng Xu,[1] Xiufang Chen,[2] Xiangang Xu,[2] Xianjin Feng[1] and Aimin Song[1,2,3]

[1]Center of Nanoelectronics and School of Microelectronics, Shandong University, Jinan 250100, China

[2]State Key Laboratory of Crystal Materials, Shandong University, Jinan 250100, China

[3]School of Electrical and Electronic Engineering, University of Manchester, Manchester M13 9PL, United Kingdom

E-mail: xianjinfeng@sdu.edu.cn and A.song@manchester.ac.uk

Abstract

GaN metal-oxide-semiconductor high-electron-mobility transistors (MOS-HEMTs) with thermally evaporated SiO gate dielectric of different thicknesses (10-30 nm) have been investigated and compared with standard metal-semiconductor HEMT (MES-HEMT). Unlike typical dielectrics for GaN MOS-HEMTs that require deposition with ion bombardments, reactive gases and/or high temperatures, thermally evaporated SiO is expected to introduce little damage to the interface. Indeed, a lower sheet resistance and higher drain current were obtained in the SiO-based MOS-HEMTs than in the MES-HEMT. In addition, significantly lower off-state drain currents and higher I_{on}/I_{off} ratios were obtained in the MOS-HEMTs. Importantly, the interface trap density in the MOS-HEMTs, ~1.0 $\times 10^{12}$ cm^{-2} eV^{-1}, was found to be significantly lower than that in MES-HEMT (2.4 $\times 10^{12}$ cm^{-2} eV^{-1}). This enables the SiO MOS-HEMTs to exhibit drastic improvements not only in the leakage currents and breakdown voltage, but also in the drain current collapse and high frequency performance. The optimized 30-nm SiO MOS-HEMT has a 438 times higher I_{on}/I_{off} ratio (1.4 $\times 10^{8}$), two orders of magnitude lower off-state drain current and gate leakage current, and 100 V higher breakdown voltage as compared to the MES-HEMT. Our study may have important implications in realizing high performance, low damage and low cost gate dielectrics for GaN HEMTs.

Keywords: GaN, MOS-HEMTs, thermal evaporation, SiO

1. Introduction

Attributed to the excellent properties of GaN, such as high breakdown field strength, high electron velocity, and good thermal stability, GaN high-electron-mobility transistors (HEMTs) have received great attention for high-frequency and high-power applications [1, 2]. Although GaN HEMT devices are very promising and significant progresses have been made in recent years, the current collapse effect and large gate leakage are still challenging issues for industrial applications of GaN HEMTs. The current collapse effect refers to a significant reduction in the drain current upon high-speed gate swings and can be alleviated by surface passivation to reduce the surface traps at the AlGaN surface [3]. Gate leakage by electron tunneling also greatly affects the power efficiency and noise performance of GaN HEMTs [4, 5]. In order to suppress the gate leakage in GaN HEMTs, recent studies have explored on the metal-insulator-semiconductor (MIS) or metal-oxide-semiconductor (MOS) structures.

GaN HEMTs that consist of a gate insulator have been shown to have an improved performance. For instance, GaN MOS-HEMTs have exhibited lower leakage current and higher breakdown voltage when compared to metal-semiconductor (MES) HEMTs [6, 7]. Different gate dielectrics such as SiN [8, 9], SiO_2 [7, 10], Al_2O_3 [11, 12], and HfO_2 [13-15] have been explored for GaN MIS-HEMTs. A variety of techniques such as plasma-enhanced chemical-vapor deposition (PECVD), atomic-layer deposition (ALD), sputtering, and molecular beam epitaxy (MBE) have been employed for the dielectric deposition [7, 8, 10-13, 16]. It is understood that the insulator-semiconductor interface traps play an important role in gate leakage [17]. However, high interface trap densities (D_{it}) ranging from 10^{12} to 10^{13} cm^{-2} eV^{-1} often occur after the insertion of gate dielectrics. For example, the measured D_{it} in PECVD-SiN_x/AlGaN [18], ALD-Al_2O_3/GaN [19] and PECVD-SiO_2/GaN [20] were 3.0×10^{12}, 1.6×10^{12}, 1.02×10^{13} cm^{-2} eV^{-1}, respectively. GaN devices are known to be sensitive to stress and increased interface traps may be introduced by high temperature deposition, reactive gases, post-deposition annealing, and ion bombardment [21-23]. Owing to free of ion bombardment, reactive gases and room-temperature deposition, SiO prepared by simple thermal evaporation has been explored in various devices [24-26]. Our recent work showed that thermally evaporated SiO can effectively reduce the current collapse effect and enhance the performance of GaN HEMTs as a surface passivation layer [27]. Nevertheless, to the best of our knowledge,

there has been no study to use thermally evaporated SiO as the gate dielectric in GaN HEMT devices.

In this work, we investigate the electrical characteristics of GaN MOS-HEMTs utilizing thermally evaporated SiO of different thicknesses as the gate dielectric. Our results show that the device performance parameters are all closely related to the thickness of SiO, such as the on-state and off-state drain currents, threshold voltage, transconductance, gate leakage current, off-state breakdown voltage, etc. Apart from improvements in the drain current, the MOS-HEMTs with a 30-nm SiO gate dielectric have exhibited about two orders of magnitude decrease in both off-state drain current (I_{off}) and gate leakage current (I_{gleak}) as well as a significant increase in breakdown voltage by ~100 V when compared to the MES-HEMT. Much lower drain current collapse, improved stability and better small signal performance are also obtained in the MOS-HEMTs as compared to the MES-HEMT, which can be explained by the much reduced interface trap density.

2. Experiments

The AlGaN/AlN/GaN heterostructure was grown by metal-organic chemical vapor deposition (MOCVD) on a 2-inch-diameter 6H-SiC substrate. The epitaxial structure consists of a 100-nm AlN nucleation layer, a 1.8-μm semi-insulating GaN buffer layer, a 1-nm AlN interlayer and a 25-nm unintentionally doped $Al_{0.22}Ga_{0.78}N$ barrier layer. A sheet carrier density (n_s) of 1.05×10^{13} cm^{-2} and a carrier mobility (μ_n) of 1810 $cm^2 \cdot V^{-1} s^{-1}$ were obtained by the Hall effect measurements at room temperature. The fabrication process of GaN MES-HEMTs started with mesa isolation by inductively coupled plasma reactive ion etching (ICP-RIE) with BCl_3/Cl_2 gas. The source and drain ohmic contacts of Ti/Al/Ni/Au (30/150/50/60 nm) were deposited by electron-beam evaporation and then annealed at 880 ^oC in N_2 for 50 s. The transmission-line method revealed an ohmic contact resistivity (ρ_c) of 3.3×10^{-6} $\Omega \cdot cm^2$ at room temperature. Finally, a Ni/Au (50/60 nm) bilayer deposited by electron-beam evaporation was used as the gate electrode. In the MOS-HEMTs fabrication, a 10, 20, or 30 nm thick SiO layer was deposited on the AlGaN surface before gate metallization. The SiO films were prepared by thermal evaporation of high purity (99.99%) SiO powders in a tungsten boat using an HHV Auto 306 thermal evaporator. After the system being pumped down, the evaporation power was increased slowly and the fresh SiO powders were carefully outgassed to ensure a stable

deposition rate. The deposition rate was 1 Å/s monitored by a quartz microbalance under a background pressure of 1 $\times 10^{-6}$ Torr. The metal electrode and SiO patterns in this work were achieved by conventional photolithography and lift-off processes. The surface morphology was examined by a Benyuan CSPM5500 atomic-force microscope (AFM) and a FEI Nova NanoSEM450 scanning electron microscope (SEM). The current-voltage (*I*-*V*), capacitance-voltage (*C*-*V*) and small signal characteristics of the HEMTs were measured using a Keysight B2902A Precision Source/Measure Unit, a Keysight E4980A Precision LCR Meter and an Agilent N5247A PNA Vector Network Analyzer at room temperature, respectively.

3. Results and discussion

Table 1. Summary of measurement results.

SiO Thickness (nm)	0	10	20	30
Gate capacitance (nF cm^{-2})	284	155	108	86
I_{dmax} (mA/mm)	317	380	402	452
R_{on} (Ω mm)	13.0	10.7	9.3	8.0
n_s (10^{12} cm^{-2})	8.1	9.6	10.8	12.1
μ_n (cm^2 V^{-1} s^{-1})	1240	1139	1090	1010
R_{sh} (Ω/sq)	620	571	529	510
I_{off} (mA/mm) @V_{gs}= -7 V	1.0×10^{-3}	6.8×10^{-5}	1.7×10^{-5}	3.8×10^{-6}
I_{on}/I_{off} ratio	3.2×10^{5}	5.6×10^{6}	2.6×10^{7}	1.4×10^{8}
V_{th} (V)	-3.4	-4.2	-5.4	-6.0
g_m (mS/mm) @V_{ds}= 10 V	110	108	90	81
SS (mV/dec)	140	121	151	164
D_{it} (10^{11} cm^{-2} eV^{-1})	23.7	9.9	10.1	9.3
Drain current collapse (%)	59	19	15	12
I_{gleak} (mA/mm) @V_{gs}= -5 V	6.4×10^{-5}	5.3×10^{-6}	2.7×10^{-6}	9.6×10^{-7}
V_{br} (V) @V_{gs}= -10 V	136	205	224	236
f_T (GHz)	2.7	3.7	5.1	6.6
f_{max} (GHz)	6.2	8.1	9.0	10.8
$f_T \cdot L_g$ (GHz μm)	5.4	7.4	10.2	13.2

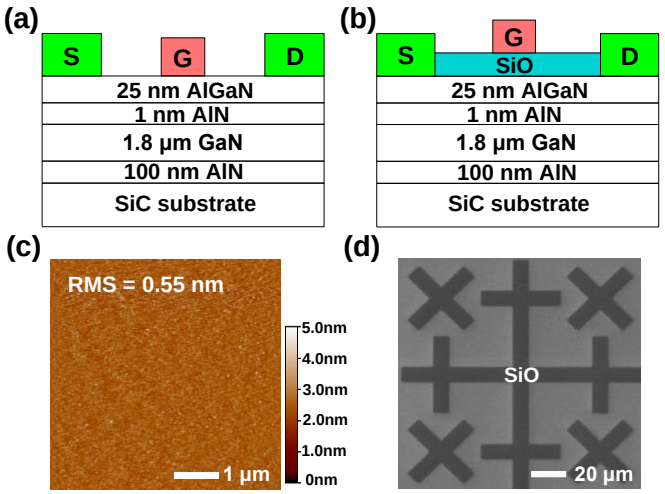

Figure 1. Schematic cross-sections of (a) the MES-HEMT and (b) the MOS-HEMTs. (c) AFM image (5 μm × 5 μm) of SiO film. (d) SEM image of SiO patterns prepared by lift-off process.

The schematic cross-sections of the MES-HEMT and the SiO MOS-HEMTs in our study are shown in Figs. 1(a) and (b), respectively. The source-drain spacing (L_{sd}) and gate-drain spacing (L_{gd}) of the devices are 14 and 6 μm, respectively. The gate length (L_g) is 2 μm and gate width (W) is 100 μm. Figure 1(c) reveals the surface topography of the 30-nm SiO film by AFM. The scan area is 5 μm × 5 μm. The SiO film prepared by thermal evaporation exhibits a smooth surface with a root-mean-square (RMS) roughness of about 0.55 nm. This value is similar to that of thermally oxidized SiO_2 [28] and is better than reported sputtered SiO_2 [7] or PECVD-SiO_x [29]. The roughness is very similar for all the SiO films of different thicknesses (10-30 nm), indicating a smooth interface between AlGaN and SiO. Moreover, the room-temperature deposition of SiO allows for the SiO patterns to be achieved through simple lift-off process as demonstrated in Fig. 1(d), hence avoiding damage to the semiconductor surface induced by the widely used dry/wet etching processes for gate dielectric patterning.

C-V measurements of the MES-HEMT and the MOS-HEMTs were performed at 1 MHz to further evaluate the SiO film properties. The *C-V* measurements were carried out using the parallel circuit mode under the bias voltage ranging from 0 to -8 V and the test pattern was 2 × 100 μm^2. Open/short/load calibration and cable length calibration were used to remove the test error introduced by the probes and cable. The zero-bias gate capacitances of MES-HEMT (C_{MES}) and MOS-HEMTs (C_{MOS}) are listed in Table 1, which summarizes the main results in our study. Assuming serial connection of AlGaN and oxide capacitors, the dielectric constant

of SiO (ε_{ox}) can be evaluated by using $C_{MOS} = C_{MES}/[1+(d_{ox}/d_s)(\varepsilon_s/\varepsilon_{ox})]$, where d_{ox} and d_s are the thicknesses of SiO and AlGaN, respectively. The dielectric constant of AlGaN (ε_s) is about 8.0 and the ε_{ox} is estimated to be 4.0, which is slightly larger than that of thermally oxidized SiO_2 (3.9).

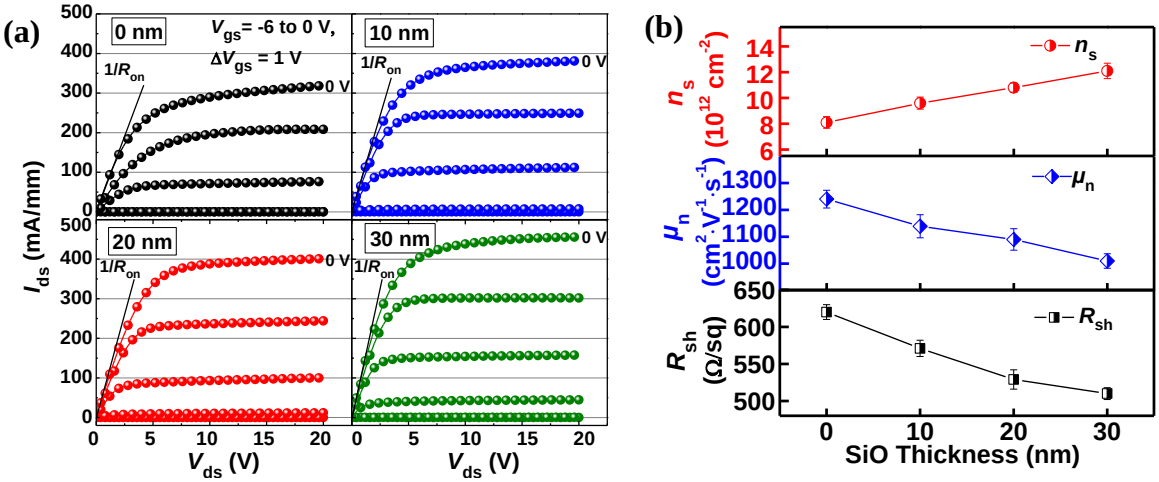

Figure 2. (a) Output characteristics and (b) sheet carrier density (n_s), electron mobility (μ_n), sheet resistance (R_{sh}) of the MES-HEMT and the MOS-HEMTs with different SiO thicknesses.

Typical output characteristics of the MES-HEMT and the MOS-HEMTs were measured at gate biases (V_{gs}) ranging from 0 V to -6 V as plotted in Fig. 2(a). All devices exhibit good saturation and pinch-off characteristics. The maximum drain current (I_{dmax}) of the MES-HEMT at zero gate bias is 317 mA/mm, while the I_{dmax} of 10, 20, and 30-nm SiO MOS-HEMTs are 380, 402, and 452 mA/mm, respectively. The higher I_{dmax} in the MOS-HEMTs may be due to the suppression of surface trapping effect by SiO passivation and/or passivation induced stress in the AlGaN layer [3, 30]. Furthermore, improved on resistance (R_{on}) of the MOS-HEMTs are found as compared to the MES-HEMT (see Table 1), implying a more conducting channel by an increased n_s.

In order to investigate the electron transport property in the channel, the n_s, μ_n and sheet resistance (R_{sh}) at zero gate bias can be calculated from the *C-V* and DC characteristics as follows [31, 32]:

$$n_s = \frac{\int_{V_{th}}^{0} C dV}{q}, \quad (1)$$

$$\mu_n = \frac{I_{ds} L_g}{q n_s W [V_{ds} - I_{ds}(R_s + R_d)]}, \quad (2)$$

$$R_{\mathrm{s}} = \frac{L_{\mathrm{gs}}}{qn_{\mathrm{s}}\mu_{\mathrm{n}}W}, \quad (3)$$

$$R_{\mathrm{d}} = \frac{L_{\mathrm{gd}}}{qn_{\mathrm{s}}\mu_{\mathrm{n}}W}, \quad (4)$$

$$R_{\mathrm{sh}} = \frac{1}{qn_{\mathrm{s}}\mu_{\mathrm{n}}}, \quad (5)$$

where V_{th} is the threshold voltage, C is the gate capacitance per unit area, V_{ds} is the drain voltage (0.1 V), R_{s} and R_{d} are the gate-source and gate-drain channel resistances, respectively. The average values of n_{s}, μ_{n} and R_{sh} with error-bars for all types of devices are summarized in Fig. 2(b). As expected, the n_{s} value of MOS-HEMTs increases significantly and ranges from 9.6 × 10^{12} to 1.21 × 10^{13} cm^{-2} when compared with that in MES-HEMT (8.1 × 10^{12} cm^{-2}), which is probably due to the reduction of surface traps [3]. Furthermore, the increased n_{s} with the increased SiO thickness could be explained by the enhanced piezoelectric polarization resulting from the SiO layer induced stress in the AlGaN layer [30]. Such a trend has also been reported for ALD-Al_2O_3 [33], MBE-SiN [16] and PECVD-SiN [9]. It has been demonstrated that the passivation layer of various thicknesses can create an addition stress which can be compressive or tensile [34, 35]. Figure 2(b) indicates a rather linear dependence of the carrier concentration on the SiO thickness, strongly suggesting a key role of the SiO-induced stress in the enhancement of the carrier concentration. Moreover, despite of slightly lower carrier mobility in the MOS-HEMTs (1139-1010 $cm^2 \cdot V^{-1} s^{-1}$) than that in the MES-HEMT (1240 $cm^2 \cdot V^{-1} s^{-1}$), all MOS-HEMTs have a more conducting channel (i.e. $1/R_{\mathrm{sh}}$) than the MES-HEMT.

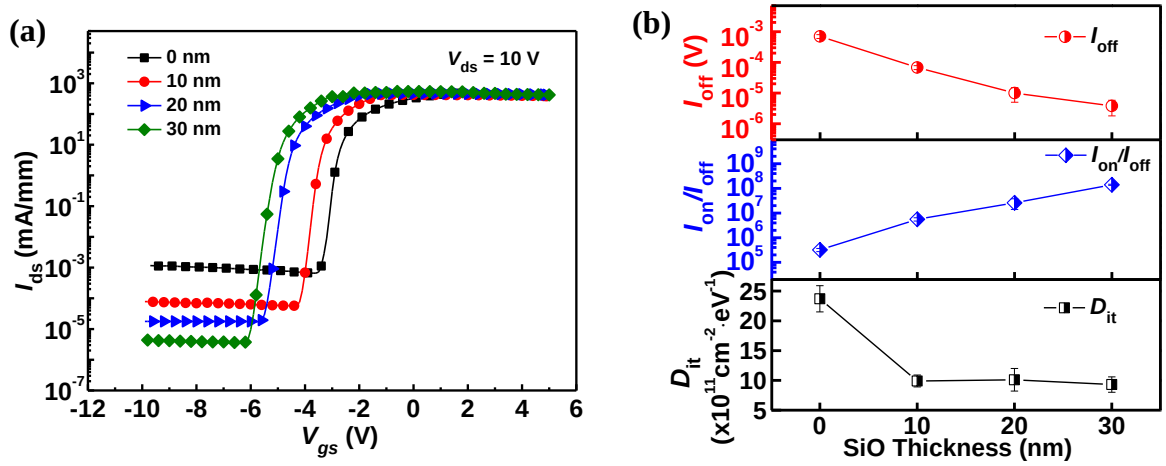

Figure 3. (a) Transfer characteristics, (b) off-state drain current (I_{off}), $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio, interface trap density (D_{it}) of the MES-HEMT and the MOS-HEMTs with different SiO thicknesses.

Figure 3(a) compares the transfer characteristics of the MES-HEMT and the MOS-HEMTs at V_{ds} = 10 V. Much lower I_{off} and much higher I_{on}/I_{off} ratio have been observed in the MOS-HEMTs than in the MES-HEMT as shown in Fig. 3(b). In particular, improvements of more than two orders of magnitude in both I_{off} and I_{on}/I_{off} ratio have been achieved in the 30-nm SiO MOS-HEMTs. In order to evaluate the interface quality, the value of D_{it} can be calculated from the subthreshold swing (*SS*) [36, 37]. The values of D_{it} in our MOS-HEMTs (9.3×10^{11}-1.01×10^{12} cm^{-2} eV^{-1}) are significantly lower than that in the MES-HEMT (2.37×10^{12} cm^{-2} eV^{-1}), and they are about ten times lower than that of reported PECVD-SiO_2-based MOS-HEMTs [20].

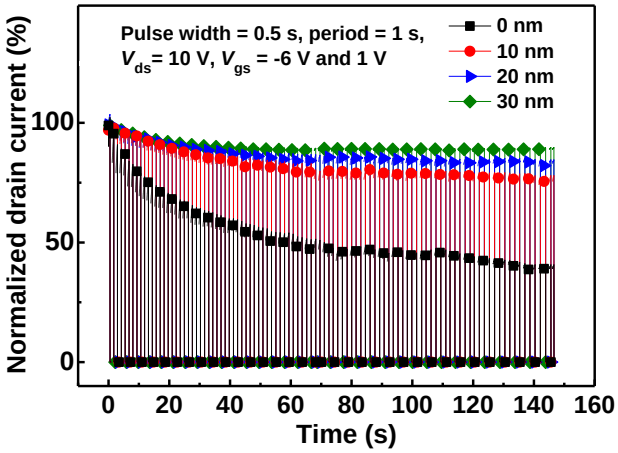

Figure 4. Transient on-off characteristics of the MES-HEMT and the MOS-HEMTs with different SiO thicknesses.

Furthermore, the transient on-off switching measurements were performed to further investigate the impact of interface traps on the device properties. The devices were switched from the off state (V_{gs} = -6 V) to the on state with a gate bias of 1V at a constant V_{ds} = 10 V. The pulse width and period of the gate bias were 0.5 and 1 s, respectively. As shown in Fig. 4, the MES-HEMT exhibits significantly higher collapse (51%) in the drain current than that of the MOS-HEMTs (12%-19%), and the most reduced current collapse effect is obtained in the devices with a 30 nm thick SiO gate dielectric. This result indicates a much reduced virtual gate effect, which agrees well with the lower trap density in MOS-HEMTs [38].

Figure 5(a) illustrates the gate leakage current in the MES-HEMT and the MOS-HEMTs. As expected, both the forward and reverse gate currents are significantly suppressed after the insertion of the SiO gate dielectric, indicating the excellent insulating properties of thermally

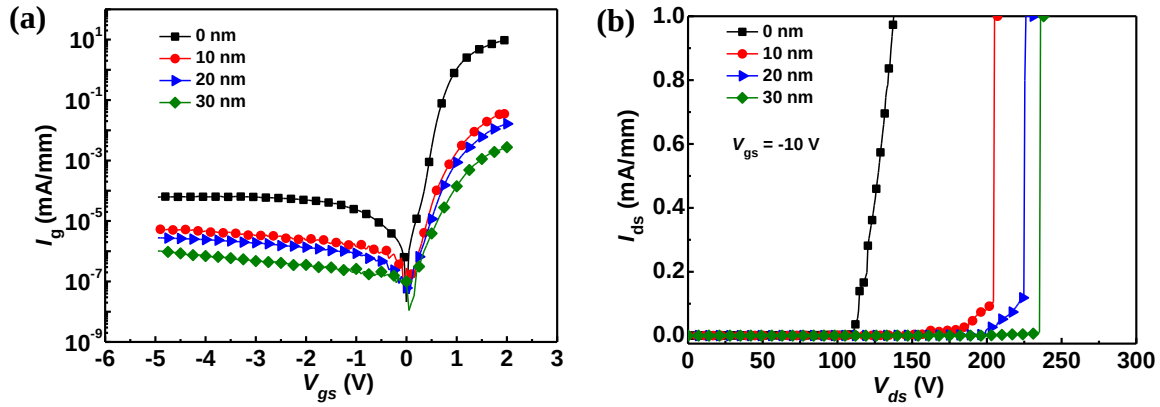

Figure 5. (a) Gate leakage current and (b) off-state breakdown characteristics of the MES-HEMT and the MOS-HEMTs.

evaporated SiO. I_{gleak} in the SiO MOS-HEMTs is up to two orders of magnitude smaller than that of the MES-HEMT at V_{gs} = -5 V, which is similar to the improvements observed in the sputtered SiN [8], ALD-Ga_2O_3 [37], sputtered HfO_2 [39] and ALD-SiO_2 [40] MOS-HEMTs. This is owing to the suppression of carrier injection between the metal gate and the semiconductor by the larger barrier height provided by the MOS structure [14, 41, 42]. Another factor that causes the large leakage current in the MES-HEMT might be the leakage paths formed by the surface states [43], which can be alleviated by passivation.

The off-state (V_{gs} = -10 V) breakdown characteristics of the devices at a drain current compliance of 1 mA/mm have also been investigated as shown in Fig. 5(b). The breakdown voltages (V_{br}) of the 10, 20, and 30-nm SiO MOS-HEMTs are 205, 224, and 236 V, respectively, significantly higher than that of the MES-HEMT (136 V). Compared with the MES-HEMT (23 V/μm), the breakdown strength (V_{br}/L_{gd}) of 30-nm SiO MOS-HEMTs is much higher (~ 39 V/μm), which is close to that of MOS-HEMTs with SiO_2, AlN and Al_2O_3 dielectrics grown by ALD [40, 44, 45]. The breakdown mechanism has been found to be caused by impact ionization which can be triggered by the gate leakage injection into the channel at high electric fields [46]. The breakdown voltage is enhanced in our MOS-HEMTs due to the suppression of gate leakage by the SiO gate dielectric [46, 47].

To investigate the small signal performance of the two types of GaN HEMTs, S-parameter measurements were carried out over the frequency ranging from 0.05 to 20 GHz at room temperature. Figure 6 plots the current gain ($|h_{21}|^2$) and maximum stable gain/maximum available gain (MSG/MAG) versus frequency of the (a) MES-HEMT and the MOS-HEMTs

with (b) 10 nm, (c) 20 nm, and (d) 30 nm SiO. During the measurements, V_{ds} was 10 V and V_{gs} set for maximum transconductance (g_m) were 0, -0.5, -1.9, and -2.6 V, respectively. Obvious increases of the current gain cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) have been observed in the MOS-HEMT devices. The f_T/f_{max} values are determined to be 2.7/6.2, 3.7/8.1, 5.1/9.0, and 6.6/10.8 GHz for the MES-HEMT, 10, 20, and 30-nm SiO MOS-HEMTs, respectively. A significant 144% increase in f_T and a 74% increase in f_{max} are achieved in the 30-nm SiO MOS-HEMTs relative to those of the MES-HEMT. The current gain cut-off frequency f_T can be approximated by $f_T = g_m/(2\pi C_{gs})$ [36], where C_{gs} is the gate capacitance. The f_T improvements in MOS-HEMTs are probably due to the larger g_m/C_{gs}, which mainly determines the cut-off frequency [48, 49]. Furthermore, the product of f_T L_g for the 30-nm SiO MOS-HEMTs is 13.2 GHz μm, which is higher than the values deduced from scaling HEMT devices [50-52]. This result is quite encouraging for HEMTs with a gate length of 2 μm and it indicates the great potential of SiO MOS-HEMTs for the high frequency applications.

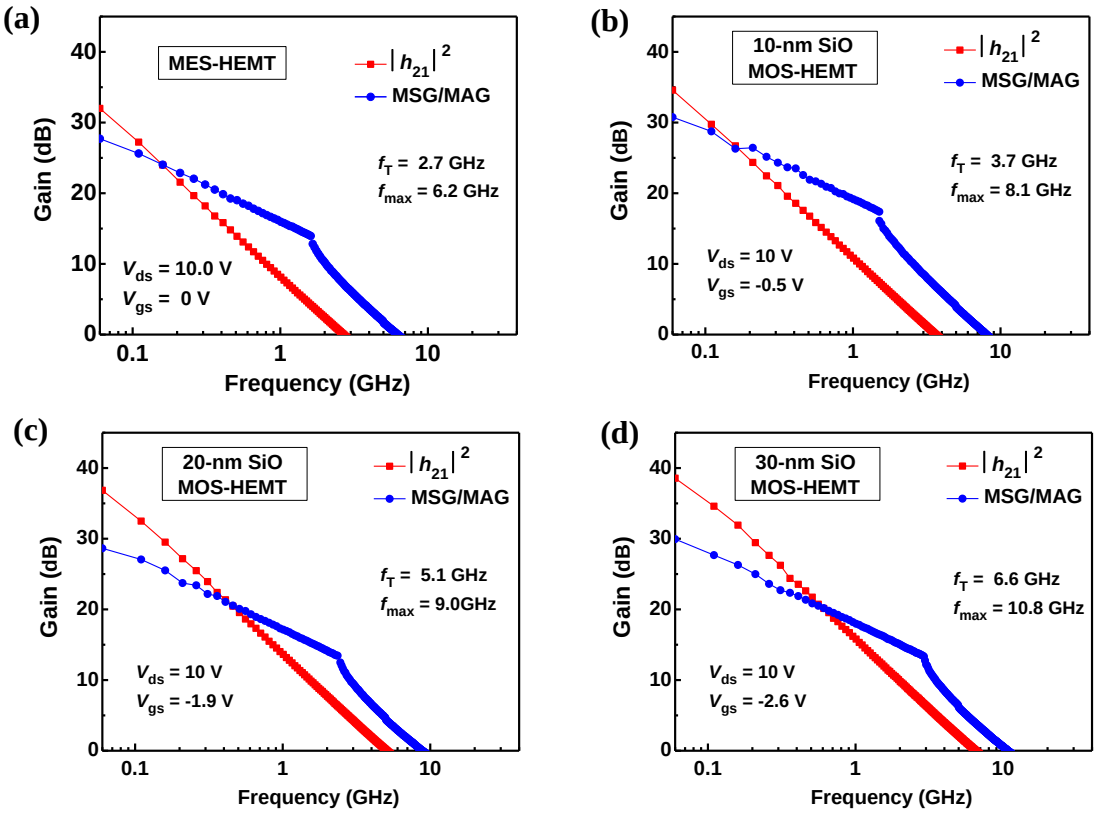

Figure 6. Small signal characteristics of the (a) MES-HEMT and the MOS-HEMTs with (b) 10 nm, (c) 20 nm, and (d) 30 nm SiO. V_{ds} was 10 V and V_{gs} set for maximum transconductance were 0, - 0.5, -1.9, and -2.6 V, respectively.

4. Conclusions

In conclusion, we have investigated the device performance of the GaN MOS-HEMTs with thermally evaporated SiO gate dielectric with different thicknesses (10-30 nm) and compared with the standard MES-HEMT. Free from any ion bombardments, high temperature, and reactive gases, the thermally evaporated SiO enabled a greatly reduced density of surface traps. Indeed, all main device performance parameters have been improved. Especially, in the MOS-HEMTs with 30-nm SiO gate dielectric, both the off-state drain current and gate leakage current decreased by about two orders of magnitude and the breakdown voltage increased by 100 V. Moreover, significant improvements of 144% in current gain cut-off frequency and 74% in maximum oscillation frequency were achieved in the 30-nm SiO MOS-HEMTs. Our results demonstrate that the low-damage, low-cost thermally evaporated SiO is a very applicable gate dielectric for GaN HEMTs.

Acknowledgments

This work was supported by National Key Research and Development Program of China (Grant Nos. 2016YFA0301200, 2016YFA0201800), National Natural Science Foundation of China (Grant No. 11374185), Engineering and Physical Sciences Research Council (EPSRC) (Grant No. EP/N021258/1), CAEP THz Science and Technology Foundation (Grant No. CAEPTHZ201409), Key Research and Development Program of Shandong Province, China (Grant Nos. 2016GGX104013, 2017GGX201007, 2016GGX4101), and Suzhou Planning Projects of Science and Technology (Grant No. SYG201616).

References

[1] K. Shinohara, D. C. Regan, Y. Tang, A. L. Corrion, D. F. Brown, J. C. Wong, J. F. Robinson, H. H. Fung, A. Schmitz, T. C. Oh, S. J. Kim, P. S. Chen, R. G. Nagele, A. D. Margomenos and M. Micovic, "Scaling of GaN HEMTs and Schottky diodes for submillimeter-wave MMIC applications," *IEEE Trans. Electron Devices* **60** (10), 2982-2996 (2013).

[2] K. Zhang, Y. Kong, G. Zhu, J. Zhou and X. Yu, "High-linearity AlGaN/GaN FinFETs for microwave power applications," *IEEE Electron Device Lett.* **38** (5), 615-618 (2017).

[3] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMT's," *IEEE Electron Device Lett.* **21** (6), 268-270 (2000).

[4] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura and T. Ogura, "High breakdown voltage undoped AlGaN–GaN power HEMT on sapphire substrate and its demonstration for DC–DC converter application,"

IEEE Trans. Electron Devices **51** (11), 1913-1917 (2004).

[5] A. V. Vertiatchikh and L. F. Eastman, "Effect of the surface and barrier defects on the AlGaN/GaN HEMT low-frequency noise performance," *IEEE Electron Device Lett.* **24** (9), 535-537 (2003).

[6] D. Meng, S. Lin, C. P. Wen, M. Wang, J. Wang, Y. Hao, Y. Zhang, K. M. Lau and W. Wu, "Low leakage current and high-cutoff frequency AlGaN/GaN MOSHEMT using submicrometer-footprint thermal oxidized TiO_2/NiO as gate dielectric" *IEEE Electron Device Lett.* **34** (6), 738-740 (2013).

[7] L. Pang, Y. Lian, D.-S. Kim, J.-H. Lee and K. Kim, "AlGaN/GaN MOSHEMT with high-quality gate-SiO_2 achieved by room-temperature radio frequency magnetron sputtering," *IEEE Trans. Electron Devices* **59** (10), 2650-2655 (2012).

[8] O. Masaru, A. Mitsutoshi, O. Yutaka, K. Shigeru, M. Kouichi and M. Takashi, "AlGaN/GaN heterostructure metal-insulator-semiconductor high-electron-mobility transistors with Si_3N_4 gate insulator", *Jpn. J. Appl. Phys*. **42** (4B), 2278-2280 (2003).

[9] S. P. Singh, Y. Liu, Y. J. Ngoo, L. M. Kyaw, M. K. Bera, S. B. Dolmanan, S. Tripathy and E. F. Chor, "Influence of PECVD deposited SiN_x passivation layer thickness on $In_{0.18}Al_{0.82}N$/GaN/Si HEMT," *J. Phys. D: Appl. Phys.* **48** (36), 365104 (2015).

[10] M. A. Khan, X. Hu, A. Tarakji, G. Simin, J. Yang, R. Gaska and M. S. Shur, "AlGaN/GaN metal-oxide-semiconductor heterostructure field-effect transistors on SiC substrates", *Appl. Phys. Lett.* **77** (9), 1339-1341 (2000).

[11] Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, K. L. Teo, S. C. Foo and V. Sahmuganathan, "Improved two-dimensional electron gas transport characteristics in AlGaN/GaN metal-insulator-semiconductor high electron mobility transistor with atomic layer-deposited Al_2O_3 as gate insulator", *Appl. Phys. Lett.* **95** (22), 223501 (2009).

[12] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder and J. C. M. Hwang, "GaN metal-oxide-semiconductor high-electron-mobility- transistor with atomic layer deposited Al_2O_3 as gate dielectric," *Appl. Phys. Lett.* **86** (6), 063501 (2005).

[13] J. Shi and L. F. Eastman, "Correlation between AlGaN/GaN MISHFET performance and HfO_2 insulation layer quality", *IEEE Electron Device Lett.* **32** (3), 312-314 (2011).

[14] C. Liu, E. F. Chor and L. S. Tan, "Investigations of HfO_2/AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors," *Appl. Phys. Lett.* **88** (17), 173504 (2006).

[15] O. Seok, W. Ahn, M.-K. Han, and M.-W. Ha, "High on/off current ratio AlGaN/GaN MOS-HEMTs employing RF-sputtered HfO_2 gate insulators," *Semicond. Sci. Technol.* **28** (2), 025001 (2013).

[16] B. P. Downey, D. J. Meyer, D. S. Katzer, T. M. Marron, M. Pan and X. Gao, "Effect of SiN_x gate insulator thickness on electrical properties of $SiN_x/In_{0.17}Al_{0.83}N$/AlN/GaN MIS–HEMTs," *Solid-State Electron.* **106**, 12-17 (2015).

[17] B. S. Eller, J. Yang and R. J. Nemanich, "Electronic surface and dielectric interface states on GaN and AlGaN," *J. Vac. Sci. Technol. A* **31** (5) (2013).

[18] Z. Tang, Q. Jiang, Y. Lu, S. Huang, S. Yang, X. Tang and K. J. Chen, "600-V normally off SiN_x/AlGaN/GaN MIS-HEMT with large gate swing and low current collapse," *IEEE Electron Device Lett.* **34** (11), 1373-1375 (2013).

[19] T.-E. Hsieh, E. Y. Chang, Y.-Z. Song, Y.-C. Lin, H.-C. Wang, S.-C. Liu, S. Salahuddin, and C. C. Hu, "Gate recessed quasi-normally OFF Al_2O_3/AlGaN/GaN MIS-HEMT with low threshold voltage hysteresis using PEALD AlN interfacial passivation layer," *IEEE Electron Device Lett.* **35** (7), 732-734 (2014).

[20] J.-P. Ao, K. Nakatani, K. Ohmuro, M. Sugimoto, C.-Y. Hu, Y. Sogawa and Y. Ohno, "GaN metal–oxide–semiconductor field-effect transistor with tetraethylorthosilicate SiO_2 gate insulator on AlGaN/GaN

heterostructure," *Jpn. J. Appl. Phys*. **49** (4), 04DF09 (2010).

[21] Y. Wu, C. Y. Chen and J. A. del Alamo, "Electrical and structural degradation of GaN high electron mobility transistors under high-power and high-temperature Direct Current stress," *J. Appl. Phys.* **117** (2), 025707 (2015).

[22] K. Eriguchi and K. Ono, "Quantitative and comparative characterizations of plasma process-induced damage in advanced metal-oxide- semiconductor devices," *J. Phys. D: Appl. Phys.* **41** (2), 024002 (2008).

[23] D. G. Kent, K. P. Lee, A. P. Zhang, B. Luo, M. E. Overberg, C. R. Abernathy, F. Ren, K. D. Mackenzie, S. J. Pearton and Y. Nakagawa, "Electrical effects of N_2 plasma exposure on dry-etch damage in p- and n-GaN Schottky diodes", *Solid-State Electron.* **45** (10), 1837-1842 (2001).

[24] H. Wang, Y. Wang, G. Zhu, Q. Wang, Q. Xin, L. Han and A. Song, "A novel thermally evaporated etching mask for low-damage dry etching," *IEEE Trans. Nanotechnol.* **16** (2), 290-295 (2017).

[25] L. Yang, H. Wang, X. Zhang, Y. Li, X. Chen, X. Xu, X. Zhao and A. Song, "Thermally evaporated SiO serving as gate dielectric in graphene field-effect transistors", *IEEE Trans. Electron Devices* **64** (4), 1846-1850 (2017).

[26] F. Zhou, H. P. Lin, L. Zhang, J. Li, X. W. Zhang, D. B. Yu, X. Y. Jiang and Z. L. Zhang, "Top-gate amorphous IGZO thin-film transistors with a SiO buffer layer inserted between active channel layer and gate insulator," *Curr. Appl. Phys.* **12** (1), 228-232 (2012).

[27] G. Zhu, H. Wang, Y. Wang, X. Feng and A. Song, "Performance enhancement of AlGaN/AlN/GaN high electron mobility transistors by thermally evaporated SiO passivation," *Appl. Phys. Lett*. **109** (11), 113503 (2016).

[28] J. Wu, Y. Chen, D. Zhou, Z. Hu, H. Xie and C. Dong, "Sputtered oxides used for passivation layers of amorphous InGaZnO thin film transistors," *Mater. Sci. Semicond. Process*. **29**, 277-282 (2014).

[29] X. Xiao, W. Deng, X. He and S. Zhang, IEEE Trans. "a-IGZO TFTs with inductively coupled plasma chemical vapor deposited SiO_x gate dielectric," *IEEE Trans. Electron Devices* **60** (8), 2687-2690 (2013).

[30] C. M. Jeon and J.-L. Lee, "Effects of tensile stress induced by silicon nitride passivation on electrical characteristics of AlGaN/GaN heterostructure field-effect transistors," *Appl. Phys. Lett.* **86** (17), 172101 (2005).

[31] Y. Lv, Z. Lin, Y. Zhang, L. Meng, C. Luan, Z. Cao, H. Chen and Z. Wang, "Polarization Coulomb field scattering in AlGaN/AlN/GaN heterostructure field-effect transistors," *Appl. Phys. Lett*. **98** (12), 123512 (2011).

[32] J. Zhao, Z. Lin, T. D. Corrigan, Z. Wang, Z. You and Z. Wang, "Electron mobility related to scattering caused by the strain variation of AlGaN barrier layer in strained AlGaN/GaN heterostructures", *Appl. Phys. Lett.* 91 (17), 173507 (2007).

[33] S. Ganguly, J. Verma, G. Li, T. Zimmermann, H. Xing and D. Jena, "Presence and origin of interface charges at atomic-layer deposited Al_2O_3/III-nitride heterojunctions," *Appl. Phys. Lett.* 99 (19), 193504 (2011).

[34] D. Gregušová, J. Bernát, M. Držík, M. Marso, J. Novák, F. Uherek and P. Kordoš, "Influence of passivation induced stress on the performance of AlGaN/GaN HEMTs," *Phys. Stat. Sol. C* **2** (7), 2619-2622 (2005).

[35] T. B. Fehlberg, J. S. Milne, G. A. Umana-Membreno, S. Keller, U. K. Mishra, B. D. Nener and G. Parish, "Transport studies of AlGaN/GaN heterostructures of different Al mole fractions with variable SiN_x passivation stress," *IEEE Trans. Electron Devices* **58** (8), 2589-2596 (2011).

[36] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices* (John Wiley & Sons, Inc., Hoboken, New Jersey, 2006) P.315.

[37] H. Y. Shih, F. C. Chu, A. Das, C. Y. Lee, M. J. Chen and R. M. Lin, "Atomic layer deposition of gallium oxide films as gate dielectrics in AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors",

Nanoscale Res. Lett. **11** (1), 235 (2016).

[38] R. Vetury, N. Q. Zhang, S. Keller and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices* **48** (3), 560-566 (2001).

[39] C. Liu, E. F. Chor, and L. S. Tan, "Enhanced device performance of AlGaN/GaN HEMTs using HfO_2 high-*k* dielectric for surface passivation and gate oxide," *Semicond. Sci. Technol.* **22** (5), 522-527 (2007).

[40] C. J. Kirkpatrick, B. Lee, R. Suri, X. Yang, and V. Misra, "Atomic layer deposition of SiO_2 for AlGaN/GaN MOS-HFETs," *IEEE Electron Device Lett.* **33** (9), 1240-1242 (2012).

[41] R. Wang, P. Saunier, Y. Tang, T. Fang, X. Gao, S. Guo, G. Snider, P. Fay, D. Jena and H. Xing, "Enhancement-mode InAlN/AlN/GaN HEMTs with 10^{-12} A/mm leakage current and 10^{12} on/off current ratio," *IEEE Electron Device Lett.* **32** (3), 309-311 (2011).

[42] P. Rottländer, M. Hehn and A. Schuhl, "Determining the interfacial barrier height and its relation to tunnel magnetoresistance", *Phys. Rev. B* **65** (5), 054422 (2002).

[43] L. Lugani, M. A. Py, J. F. Carlin and N. Grandjean, "Leakage mechanisms in InAlN based heterostructures," *J. Appl. Phys.* **115** (7), 074506 (2014).

[44] X. Y. Liu, S. X. Zhao, L. Q. Zhang, H. F. Huang, J. S. Shi, C. M. Zhang, H. L. Lu, P. F. Wang, and D. W. Zhang, "AlGaN/GaN MISHEMTs with AlN gate dielectric grown by thermal ALD technique," *Nanoscale Res. Lett.* **10**, 109 (2015).

[45] J. J. Freedsman, T. Kubo, and T. Egawa, "High drain current density E-mode Al_2O_3/AlGaN/GaN MOS-HEMT on Si with enhanced power device figure-of-merit," *IEEE Trans. Electron Devices* **60** (10), 3079-3083 (2013).

[46] T. Nakao, Y. Ohno, S. Kishimoto, K. Maezawa and T. Mizutani, "Study on off-state breakdown in AlGaN/GaN HEMTs," *Phys. Stat. Sol. C* **0** (7), 2335-2338 (2003).

[47] Y. Ohno, T. Nakao, S. Kishimoto, K. Maezawa and T. Mizutani, "Effects of surface passivation on breakdown of AlGaN/GaN high-electron- mobility transistors," *Appl. Phys. Lett.* **84** (12), 2184 (2004).

[48] C. K. Wang, R. W. Chuang, S. J. Chang, Y. K. Su, S. C. Wei, T. K. Lin, T. K. Ko, Y. Z. Chiou, and J. J. Tang, "High temperature and high frequency characteristics of AlGaN/GaN MOS-HFETs with photochemical vapor deposition SiO_2 layer," *Mat. Sci. Eng. B* **119** (1), 25-28 (2005).

[49] K.-W. Lee, K.-L. Lee, X.-Z. Lin, C.-H. Tu, and Y.-H. Wang, "Improvement of impact ionization effect and subthreshold current in InAlAs/InGaAs metal-oxide-semiconductor metamorphic HEMT with a liquid-phase oxidized InAlAs as gate insulator," *IEEE Trans. Electron Devices* **54** (3), 418-424 (2007).

[50] M. A. Alim, A. A. Rezazadeh, and C. Gaquiere, "Thermal characterization of DC and small-signal parameters of 150 nm and 250 nm gate-length AlGaN/GaN HEMTs grown on a SiC substrate," *Semicond. Sci. Technol.* **30** (12), 125005 (2015).

[51] G. Crupi, G. Avolio, A. Raffo, P. Barmuta, D. M. M. P. Schreurs, A. Caddemi, and G. Vannini, "Investigation on the thermal behavior of microwave GaN HEMTs," *Solid-State Electron*. **64** (1), 28-33 (2011).

[52] J.-S. Shi, H.-F. Huang, X.-Y. Liu, S.-X. Zhao, L.-Q. Zhang, and P.-F. Wang, "Effect of device geometry on static and dynamic performance of AlGaN/GaN-on-Si high electron mobility transistor," *Mater. Res. Express* **3** (8), 085013 (2016).

GaN metal-oxide-semiconductor high-electron-mobility transistors using thermally evaporated SiO as the gate dielectric

Gengchang Zhu,[1] Yiming Wang,[1] Qian Xin,[1,2] Mingsheng Xu,[1] Xiufang Chen,[2] Xiangang Xu,[2] Xianjin Feng[1] and Aimin Song[1,2,3]

[1]Center of Nanoelectronics and School of Microelectronics, Shandong University, Jinan 250100, China

[2]State Key Laboratory of Crystal Materials, Shandong University, Jinan 250100, China

[3]School of Electrical and Electronic Engineering, University of Manchester, Manchester M13 9PL, United Kingdom

E-mail: xianjinfeng@sdu.edu.cn and A.song@manchester.ac.uk

Abstract

GaN metal-oxide-semiconductor high-electron-mobility transistors (MOS-HEMTs) with thermally evaporated SiO gate dielectric of different thicknesses (10-30 nm) have been investigated and compared with standard metal-semiconductor HEMT (MES-HEMT). Unlike typical dielectrics for GaN MOS-HEMTs that require deposition with ion bombardments, reactive gases and/or high temperatures, thermally evaporated SiO is expected to introduce little damage to the interface. Indeed, a lower sheet resistance and higher drain current were obtained in the SiO-based MOS-HEMTs than in the MES-HEMT. In addition, significantly lower off-state drain currents and higher I_{on}/I_{off} ratios were obtained in the MOS-HEMTs. Importantly, the interface trap density in the MOS-HEMTs, ~1.0 $\times 10^{12}$ cm^{-2} eV^{-1}, was found to be significantly lower than that in MES-HEMT (2.4 $\times 10^{12}$ cm^{-2} eV^{-1}). This enables the SiO MOS-HEMTs to exhibit drastic improvements not only in the leakage currents and breakdown voltage, but also in the drain current collapse and high frequency performance. The optimized 30-nm SiO MOS-HEMT has a 438 times higher I_{on}/I_{off} ratio (1.4 $\times 10^{8}$), two orders of magnitude lower off-state drain current and gate leakage current, and 100 V higher breakdown voltage as compared to the MES-HEMT. Our study may have important implications in realizing high performance, low damage and low cost gate dielectrics for GaN HEMTs.

Keywords: GaN, MOS-HEMTs, thermal evaporation, SiO

1. Introduction

Attributed to the excellent properties of GaN, such as high breakdown field strength, high electron velocity, and good thermal stability, GaN high-electron-mobility transistors (HEMTs) have received great attention for high-frequency and high-power applications [1, 2]. Although GaN HEMT devices are very promising and significant progresses have been made in recent years, the current collapse effect and large gate leakage are still challenging issues for industrial applications of GaN HEMTs. The current collapse effect refers to a significant reduction in the drain current upon high-speed gate swings and can be alleviated by surface passivation to reduce the surface traps at the AlGaN surface [3]. Gate leakage by electron tunneling also greatly affects the power efficiency and noise performance of GaN HEMTs [4, 5]. In order to suppress the gate leakage in GaN HEMTs, recent studies have explored on the metal-insulator-semiconductor (MIS) or metal-oxide-semiconductor (MOS) structures.

GaN HEMTs that consist of a gate insulator have been shown to have an improved performance. For instance, GaN MOS-HEMTs have exhibited lower leakage current and higher breakdown voltage when compared to metal-semiconductor (MES) HEMTs [6, 7]. Different gate dielectrics such as SiN [8, 9], SiO_2 [7, 10], Al_2O_3 [11, 12], and HfO_2 [13-15] have been explored for GaN MIS-HEMTs. A variety of techniques such as plasma-enhanced chemical-vapor deposition (PECVD), atomic-layer deposition (ALD), sputtering, and molecular beam epitaxy (MBE) have been employed for the dielectric deposition [7, 8, 10-13, 16]. It is understood that the insulator-semiconductor interface traps play an important role in gate leakage [17]. However, high interface trap densities (D_{it}) ranging from 10^{12} to 10^{13} cm^{-2} eV^{-1} often occur after the insertion of gate dielectrics. For example, the measured D_{it} in PECVD-SiN_x/AlGaN [18], ALD-Al_2O_3/GaN [19] and PECVD-SiO_2/GaN [20] were 3.0×10^{12}, 1.6×10^{12}, 1.02×10^{13} cm^{-2} eV^{-1}, respectively. GaN devices are known to be sensitive to stress and increased interface traps may be introduced by high temperature deposition, reactive gases, post-deposition annealing, and ion bombardment [21-23]. Owing to free of ion bombardment, reactive gases and room-temperature deposition, SiO prepared by simple thermal evaporation has been explored in various devices [24-26]. Our recent work showed that thermally evaporated SiO can effectively reduce the current collapse effect and enhance the performance of GaN HEMTs as a surface passivation layer [27]. Nevertheless, to the best of our knowledge,

there has been no study to use thermally evaporated SiO as the gate dielectric in GaN HEMT devices.

In this work, we investigate the electrical characteristics of GaN MOS-HEMTs utilizing thermally evaporated SiO of different thicknesses as the gate dielectric. Our results show that the device performance parameters are all closely related to the thickness of SiO, such as the on-state and off-state drain currents, threshold voltage, transconductance, gate leakage current, off-state breakdown voltage, etc. Apart from improvements in the drain current, the MOS-HEMTs with a 30-nm SiO gate dielectric have exhibited about two orders of magnitude decrease in both off-state drain current (I_{off}) and gate leakage current (I_{gleak}) as well as a significant increase in breakdown voltage by ~100 V when compared to the MES-HEMT. Much lower drain current collapse, improved stability and better small signal performance are also obtained in the MOS-HEMTs as compared to the MES-HEMT, which can be explained by the much reduced interface trap density.

2. Experiments

The AlGaN/AlN/GaN heterostructure was grown by metal-organic chemical vapor deposition (MOCVD) on a 2-inch-diameter 6H-SiC substrate. The epitaxial structure consists of a 100-nm AlN nucleation layer, a 1.8-μm semi-insulating GaN buffer layer, a 1-nm AlN interlayer and a 25-nm unintentionally doped $Al_{0.22}Ga_{0.78}N$ barrier layer. A sheet carrier density (n_s) of 1.05×10^{13} cm^{-2} and a carrier mobility (μ_n) of 1810 $cm^2 \cdot V^{-1} s^{-1}$ were obtained by the Hall effect measurements at room temperature. The fabrication process of GaN MES-HEMTs started with mesa isolation by inductively coupled plasma reactive ion etching (ICP-RIE) with BCl_3/Cl_2 gas. The source and drain ohmic contacts of Ti/Al/Ni/Au (30/150/50/60 nm) were deposited by electron-beam evaporation and then annealed at 880 °C in N_2 for 50 s. The transmission-line method revealed an ohmic contact resistivity (ρ_c) of 3.3×10^{-6} $\Omega \cdot cm^2$ at room temperature. Finally, a Ni/Au (50/60 nm) bilayer deposited by electron-beam evaporation was used as the gate electrode. In the MOS-HEMTs fabrication, a 10, 20, or 30 nm thick SiO layer was deposited on the AlGaN surface before gate metallization. The SiO films were prepared by thermal evaporation of high purity (99.99%) SiO powders in a tungsten boat using an HHV Auto 306 thermal evaporator. After the system being pumped down, the evaporation power was increased slowly and the fresh SiO powders were carefully outgassed to ensure a stable

deposition rate. The deposition rate was 1 Å/s monitored by a quartz microbalance under a background pressure of 1 $\times 10^{-6}$ Torr. The metal electrode and SiO patterns in this work were achieved by conventional photolithography and lift-off processes. The surface morphology was examined by a Benyuan CSPM5500 atomic-force microscope (AFM) and a FEI Nova NanoSEM450 scanning electron microscope (SEM). The current-voltage (*I*-*V*), capacitance-voltage (*C*-*V*) and small signal characteristics of the HEMTs were measured using a Keysight B2902A Precision Source/Measure Unit, a Keysight E4980A Precision LCR Meter and an Agilent N5247A PNA Vector Network Analyzer at room temperature, respectively.

3. Results and discussion

Table 1. Summary of measurement results.

SiO Thickness (nm)	0	10	20	30
Gate capacitance (nF cm^{-2})	284	155	108	86
I_{dmax} (mA/mm)	317	380	402	452
R_{on} (Ω mm)	13.0	10.7	9.3	8.0
n_s (10^{12} cm^{-2})	8.1	9.6	10.8	12.1
μ_n (cm^2 V^{-1} s^{-1})	1240	1139	1090	1010
R_{sh} (Ω/sq)	620	571	529	510
I_{off} (mA/mm) @V_{gs}= -7 V	1.0 $\times 10^{-3}$	6.8 $\times 10^{-5}$	1.7 $\times 10^{-5}$	3.8 $\times 10^{-6}$
I_{on}/I_{off} ratio	3.2 $\times 10^{5}$	5.6 $\times 10^{6}$	2.6 $\times 10^{7}$	1.4 $\times 10^{8}$
V_{th} (V)	-3.4	-4.2	-5.4	-6.0
g_m (mS/mm) @V_{ds}= 10 V	110	108	90	81
SS (mV/dec)	140	121	151	164
D_{it} (10^{11} cm^{-2} eV^{-1})	23.7	9.9	10.1	9.3
Drain current collapse (%)	59	19	15	12
I_{gleak} (mA/mm) @V_{gs}= -5 V	6.4 $\times 10^{-5}$	5.3 $\times 10^{-6}$	2.7 $\times 10^{-6}$	9.6 $\times 10^{-7}$
V_{br} (V) @V_{gs}= -10 V	136	205	224	236
f_T (GHz)	2.7	3.7	5.1	6.6
f_{max} (GHz)	6.2	8.1	9.0	10.8
f_T L_g (GHz μm)	5.4	7.4	10.2	13.2

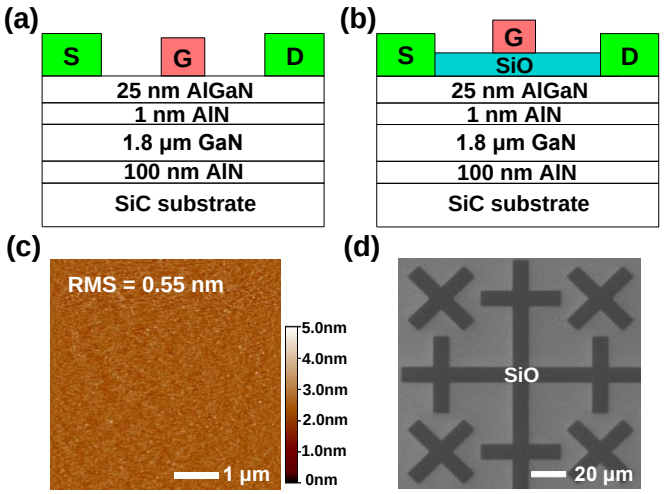

Figure 1. Schematic cross-sections of (a) the MES-HEMT and (b) the MOS-HEMTs. (c) AFM image (5 μm × 5 μm) of SiO film. (d) SEM image of SiO patterns prepared by lift-off process.

The schematic cross-sections of the MES-HEMT and the SiO MOS-HEMTs in our study are shown in Figs. 1(a) and (b), respectively. The source-drain spacing (L_{sd}) and gate-drain spacing (L_{gd}) of the devices are 14 and 6 μm, respectively. The gate length (L_g) is 2 μm and gate width (W) is 100 μm. Figure 1(c) reveals the surface topography of the 30-nm SiO film by AFM. The scan area is 5 μm × 5 μm. The SiO film prepared by thermal evaporation exhibits a smooth surface with a root-mean-square (RMS) roughness of about 0.55 nm. This value is similar to that of thermally oxidized SiO_2 [28] and is better than reported sputtered SiO_2 [7] or PECVD-SiO_x [29]. The roughness is very similar for all the SiO films of different thicknesses (10-30 nm), indicating a smooth interface between AlGaN and SiO. Moreover, the room-temperature deposition of SiO allows for the SiO patterns to be achieved through simple lift-off process as demonstrated in Fig. 1(d), hence avoiding damage to the semiconductor surface induced by the widely used dry/wet etching processes for gate dielectric patterning.

C-V measurements of the MES-HEMT and the MOS-HEMTs were performed at 1 MHz to further evaluate the SiO film properties. The *C-V* measurements were carried out using the parallel circuit mode under the bias voltage ranging from 0 to -8 V and the test pattern was 2 × 100 μm^2. Open/short/load calibration and cable length calibration were used to remove the test error introduced by the probes and cable. The zero-bias gate capacitances of MES-HEMT (C_{MES}) and MOS-HEMTs (C_{MOS}) are listed in Table 1, which summarizes the main results in our study. Assuming serial connection of AlGaN and oxide capacitors, the dielectric constant

of SiO (ε_{ox}) can be evaluated by using $C_{MOS} = C_{MES}/[1+(d_{ox}/d_s)(\varepsilon_s/\varepsilon_{ox})]$, where d_{ox} and d_s are the thicknesses of SiO and AlGaN, respectively. The dielectric constant of AlGaN (ε_s) is about 8.0 and the ε_{ox} is estimated to be 4.0, which is slightly larger than that of thermally oxidized SiO_2 (3.9).

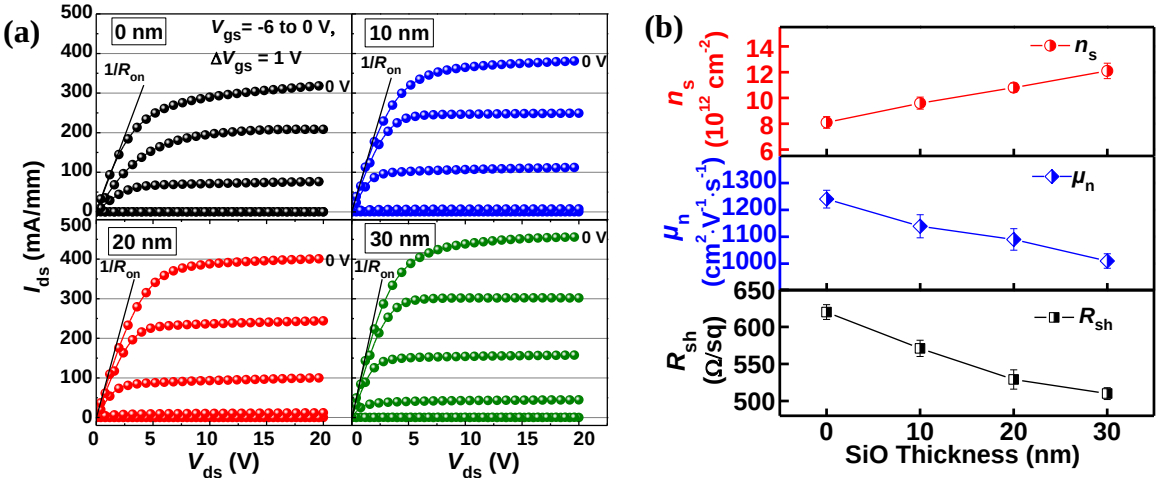

Figure 2. (a) Output characteristics and (b) sheet carrier density (n_s), electron mobility (μ_n), sheet resistance (R_{sh}) of the MES-HEMT and the MOS-HEMTs with different SiO thicknesses.

Typical output characteristics of the MES-HEMT and the MOS-HEMTs were measured at gate biases (V_{gs}) ranging from 0 V to -6 V as plotted in Fig. 2(a). All devices exhibit good saturation and pinch-off characteristics. The maximum drain current (I_{dmax}) of the MES-HEMT at zero gate bias is 317 mA/mm, while the I_{dmax} of 10, 20, and 30-nm SiO MOS-HEMTs are 380, 402, and 452 mA/mm, respectively. The higher I_{dmax} in the MOS-HEMTs may be due to the suppression of surface trapping effect by SiO passivation and/or passivation induced stress in the AlGaN layer [3, 30]. Furthermore, improved on resistance (R_{on}) of the MOS-HEMTs are found as compared to the MES-HEMT (see Table 1), implying a more conducting channel by an increased n_s.

In order to investigate the electron transport property in the channel, the n_s, μ_n and sheet resistance (R_{sh}) at zero gate bias can be calculated from the *C-V* and DC characteristics as follows [31, 32]:

$$n_s = \frac{\int_{V_{th}}^{0} C dV}{q}, \quad (1)$$

$$\mu_n = \frac{I_{ds} L_g}{q n_s W [V_{ds} - I_{ds}(R_s + R_d)]}, \quad (2)$$

$$R_{\mathrm{s}} = \frac{L_{\mathrm{gs}}}{qn_{\mathrm{s}}\mu_{\mathrm{n}}W}, \quad (3)$$

$$R_{\mathrm{d}} = \frac{L_{\mathrm{gd}}}{qn_{\mathrm{s}}\mu_{\mathrm{n}}W}, \quad (4)$$

$$R_{\mathrm{sh}} = \frac{1}{qn_{\mathrm{s}}\mu_{\mathrm{n}}}, \quad (5)$$

where V_{th} is the threshold voltage, C is the gate capacitance per unit area, V_{ds} is the drain voltage (0.1 V), R_{s} and R_{d} are the gate-source and gate-drain channel resistances, respectively. The average values of n_{s}, μ_{n} and R_{sh} with error-bars for all types of devices are summarized in Fig. 2(b). As expected, the n_{s} value of MOS-HEMTs increases significantly and ranges from 9.6 × 10^{12} to 1.21 × 10^{13} cm^{-2} when compared with that in MES-HEMT (8.1 × 10^{12} cm^{-2}), which is probably due to the reduction of surface traps [3]. Furthermore, the increased n_{s} with the increased SiO thickness could be explained by the enhanced piezoelectric polarization resulting from the SiO layer induced stress in the AlGaN layer [30]. Such a trend has also been reported for ALD-Al_2O_3 [33], MBE-SiN [16] and PECVD-SiN [9]. It has been demonstrated that the passivation layer of various thicknesses can create an addition stress which can be compressive or tensile [34, 35]. Figure 2(b) indicates a rather linear dependence of the carrier concentration on the SiO thickness, strongly suggesting a key role of the SiO-induced stress in the enhancement of the carrier concentration. Moreover, despite of slightly lower carrier mobility in the MOS-HEMTs (1139-1010 $cm^2 \cdot V^{-1} s^{-1}$) than that in the MES-HEMT (1240 $cm^2 \cdot V^{-1} s^{-1}$), all MOS-HEMTs have a more conducting channel (i.e. $1/R_{\mathrm{sh}}$) than the MES-HEMT.

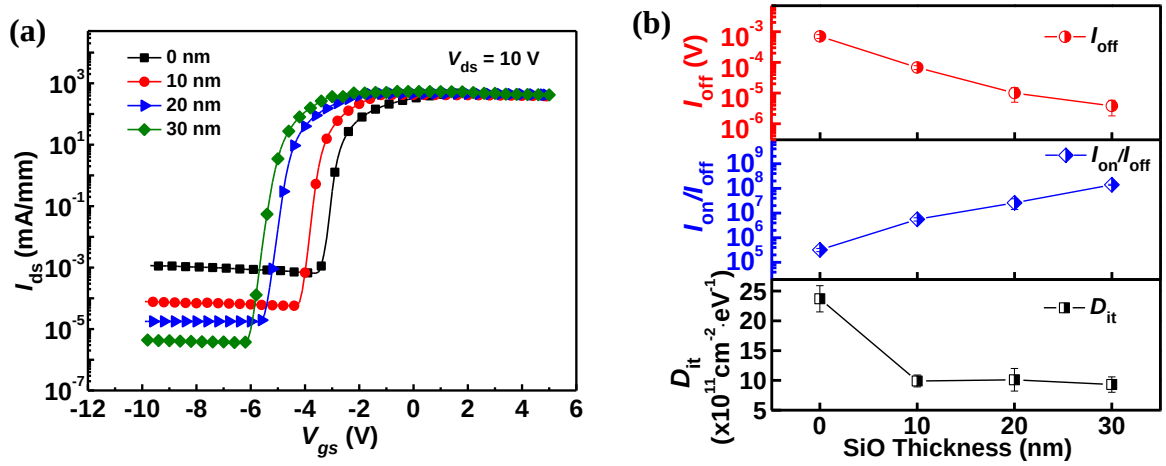

Figure 3. (a) Transfer characteristics, (b) off-state drain current (I_{off}), $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio, interface trap density (D_{it}) of the MES-HEMT and the MOS-HEMTs with different SiO thicknesses.

Figure 3(a) compares the transfer characteristics of the MES-HEMT and the MOS-HEMTs at V_{ds} = 10 V. Much lower I_{off} and much higher I_{on}/I_{off} ratio have been observed in the MOS-HEMTs than in the MES-HEMT as shown in Fig. 3(b). In particular, improvements of more than two orders of magnitude in both I_{off} and I_{on}/I_{off} ratio have been achieved in the 30-nm SiO MOS-HEMTs. In order to evaluate the interface quality, the value of D_{it} can be calculated from the subthreshold swing (*SS*) [36, 37]. The values of D_{it} in our MOS-HEMTs (9.3×10^{11}-1.01×10^{12} cm^{-2} eV^{-1}) are significantly lower than that in the MES-HEMT (2.37×10^{12} cm^{-2} eV^{-1}), and they are about ten times lower than that of reported PECVD-SiO_2-based MOS-HEMTs [20].

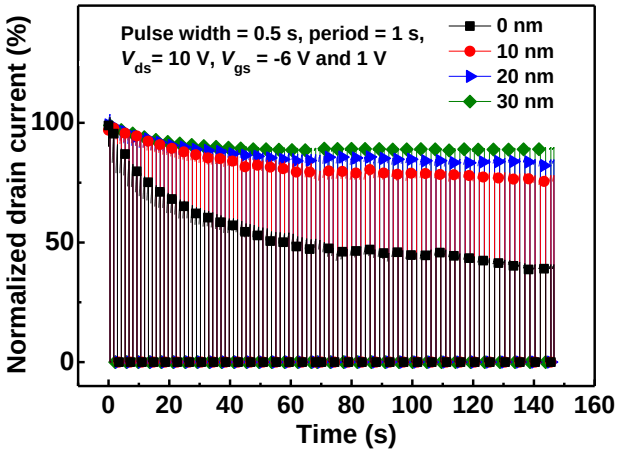

Figure 4. Transient on-off characteristics of the MES-HEMT and the MOS-HEMTs with different SiO thicknesses.

Furthermore, the transient on-off switching measurements were performed to further investigate the impact of interface traps on the device properties. The devices were switched from the off state (V_{gs} = -6 V) to the on state with a gate bias of 1V at a constant V_{ds} = 10 V. The pulse width and period of the gate bias were 0.5 and 1 s, respectively. As shown in Fig. 4, the MES-HEMT exhibits significantly higher collapse (51%) in the drain current than that of the MOS-HEMTs (12%-19%), and the most reduced current collapse effect is obtained in the devices with a 30 nm thick SiO gate dielectric. This result indicates a much reduced virtual gate effect, which agrees well with the lower trap density in MOS-HEMTs [38].

Figure 5(a) illustrates the gate leakage current in the MES-HEMT and the MOS-HEMTs. As expected, both the forward and reverse gate currents are significantly suppressed after the insertion of the SiO gate dielectric, indicating the excellent insulating properties of thermally

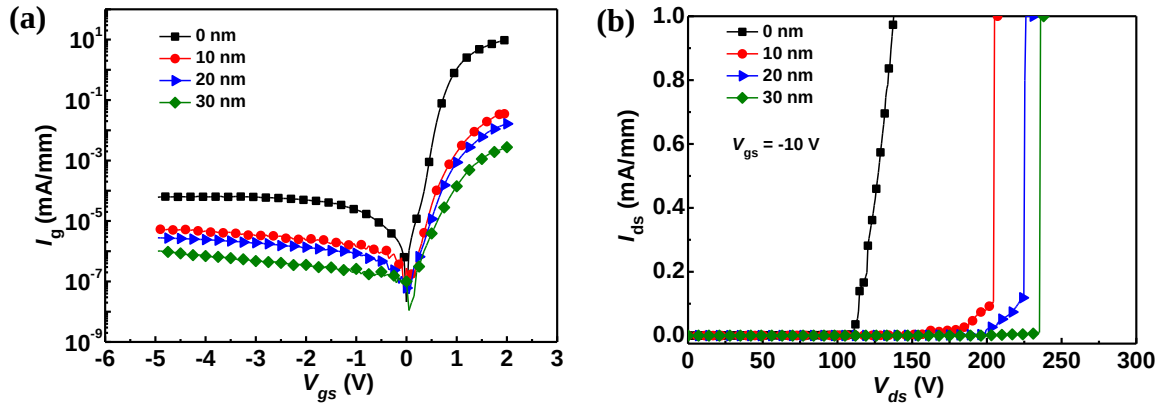

Figure 5. (a) Gate leakage current and (b) off-state breakdown characteristics of the MES-HEMT and the MOS-HEMTs.

evaporated SiO. I_{gleak} in the SiO MOS-HEMTs is up to two orders of magnitude smaller than that of the MES-HEMT at V_{gs} = -5 V, which is similar to the improvements observed in the sputtered SiN [8], ALD-Ga_2O_3 [37], sputtered HfO_2 [39] and ALD-SiO_2 [40] MOS-HEMTs. This is owing to the suppression of carrier injection between the metal gate and the semiconductor by the larger barrier height provided by the MOS structure [14, 41, 42]. Another factor that causes the large leakage current in the MES-HEMT might be the leakage paths formed by the surface states [43], which can be alleviated by passivation.

The off-state (V_{gs} = -10 V) breakdown characteristics of the devices at a drain current compliance of 1 mA/mm have also been investigated as shown in Fig. 5(b). The breakdown voltages (V_{br}) of the 10, 20, and 30-nm SiO MOS-HEMTs are 205, 224, and 236 V, respectively, significantly higher than that of the MES-HEMT (136 V). Compared with the MES-HEMT (23 V/μm), the breakdown strength (V_{br}/L_{gd}) of 30-nm SiO MOS-HEMTs is much higher (~ 39 V/μm), which is close to that of MOS-HEMTs with SiO_2, AlN and Al_2O_3 dielectrics grown by ALD [40, 44, 45]. The breakdown mechanism has been found to be caused by impact ionization which can be triggered by the gate leakage injection into the channel at high electric fields [46]. The breakdown voltage is enhanced in our MOS-HEMTs due to the suppression of gate leakage by the SiO gate dielectric [46, 47].

To investigate the small signal performance of the two types of GaN HEMTs, S-parameter measurements were carried out over the frequency ranging from 0.05 to 20 GHz at room temperature. Figure 6 plots the current gain ($|h_{21}|^2$) and maximum stable gain/maximum available gain (MSG/MAG) versus frequency of the (a) MES-HEMT and the MOS-HEMTs

with (b) 10 nm, (c) 20 nm, and (d) 30 nm SiO. During the measurements, V_{ds} was 10 V and V_{gs} set for maximum transconductance (g_m) were 0, -0.5, -1.9, and -2.6 V, respectively. Obvious increases of the current gain cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) have been observed in the MOS-HEMT devices. The f_T/f_{max} values are determined to be 2.7/6.2, 3.7/8.1, 5.1/9.0, and 6.6/10.8 GHz for the MES-HEMT, 10, 20, and 30-nm SiO MOS-HEMTs, respectively. A significant 144% increase in f_T and a 74% increase in f_{max} are achieved in the 30-nm SiO MOS-HEMTs relative to those of the MES-HEMT. The current gain cut-off frequency f_T can be approximated by $f_T = g_m/(2\pi C_{gs})$ [36], where C_{gs} is the gate capacitance. The f_T improvements in MOS-HEMTs are probably due to the larger g_m/C_{gs}, which mainly determines the cut-off frequency [48, 49]. Furthermore, the product of f_T L_g for the 30-nm SiO MOS-HEMTs is 13.2 GHz μm, which is higher than the values deduced from scaling HEMT devices [50-52]. This result is quite encouraging for HEMTs with a gate length of 2 μm and it indicates the great potential of SiO MOS-HEMTs for the high frequency applications.

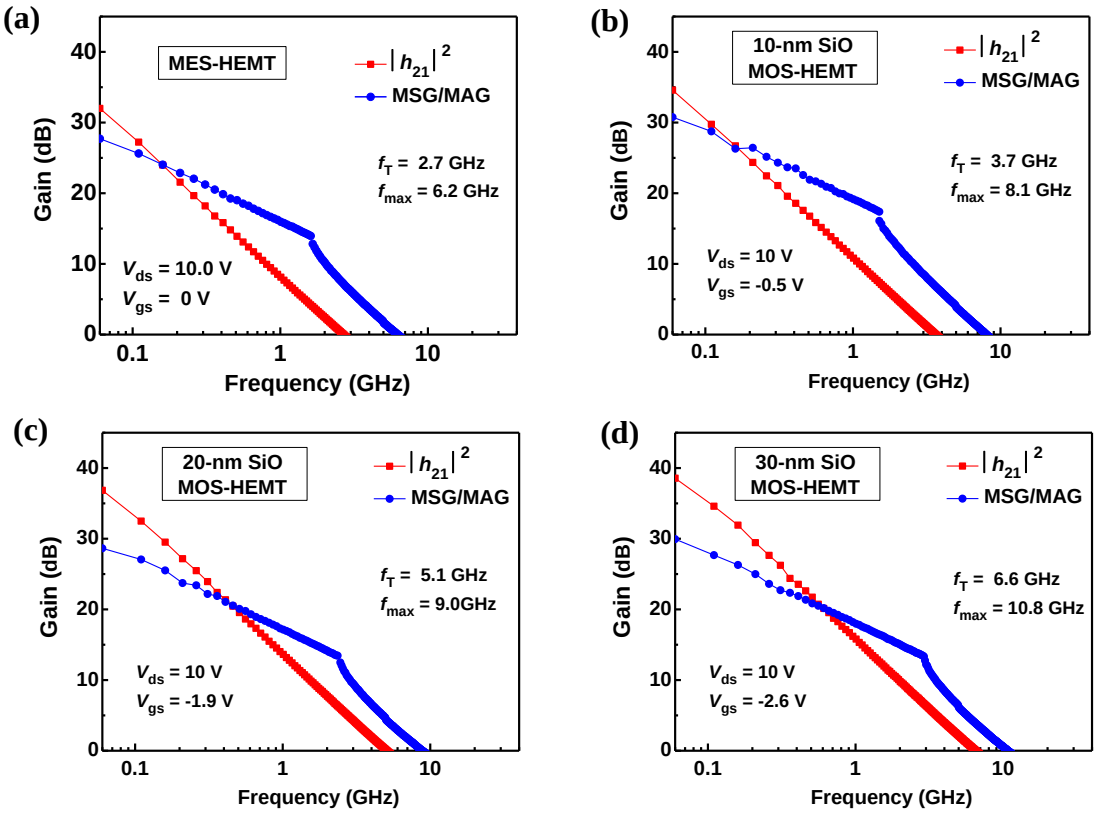

Figure 6. Small signal characteristics of the (a) MES-HEMT and the MOS-HEMTs with (b) 10 nm, (c) 20 nm, and (d) 30 nm SiO. V_{ds} was 10 V and V_{gs} set for maximum transconductance were 0, - 0.5, -1.9, and -2.6 V, respectively.

4. Conclusions

In conclusion, we have investigated the device performance of the GaN MOS-HEMTs with thermally evaporated SiO gate dielectric with different thicknesses (10-30 nm) and compared with the standard MES-HEMT. Free from any ion bombardments, high temperature, and reactive gases, the thermally evaporated SiO enabled a greatly reduced density of surface traps. Indeed, all main device performance parameters have been improved. Especially, in the MOS-HEMTs with 30-nm SiO gate dielectric, both the off-state drain current and gate leakage current decreased by about two orders of magnitude and the breakdown voltage increased by 100 V. Moreover, significant improvements of 144% in current gain cut-off frequency and 74% in maximum oscillation frequency were achieved in the 30-nm SiO MOS-HEMTs. Our results demonstrate that the low-damage, low-cost thermally evaporated SiO is a very applicable gate dielectric for GaN HEMTs.

Acknowledgments

This work was supported by National Key Research and Development Program of China (Grant Nos. 2016YFA0301200, 2016YFA0201800), National Natural Science Foundation of China (Grant No. 11374185), Engineering and Physical Sciences Research Council (EPSRC) (Grant No. EP/N021258/1), CAEP THz Science and Technology Foundation (Grant No. CAEPTHZ201409), Key Research and Development Program of Shandong Province, China (Grant Nos. 2016GGX104013, 2017GGX201007, 2016GGX4101), and Suzhou Planning Projects of Science and Technology (Grant No. SYG201616).

References

[1] K. Shinohara, D. C. Regan, Y. Tang, A. L. Corrion, D. F. Brown, J. C. Wong, J. F. Robinson, H. H. Fung, A. Schmitz, T. C. Oh, S. J. Kim, P. S. Chen, R. G. Nagele, A. D. Margomenos and M. Micovic, "Scaling of GaN HEMTs and Schottky diodes for submillimeter-wave MMIC applications," *IEEE Trans. Electron Devices* **60** (10), 2982-2996 (2013).

[2] K. Zhang, Y. Kong, G. Zhu, J. Zhou and X. Yu, "High-linearity AlGaN/GaN FinFETs for microwave power applications," *IEEE Electron Device Lett.* **38** (5), 615-618 (2017).

[3] B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy and L. F. Eastman, "The effect of surface passivation on the microwave characteristics of undoped AlGaN/GaN HEMT's," *IEEE Electron Device Lett.* **21** (6), 268-270 (2000).

[4] W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, I. Omura and T. Ogura, "High breakdown voltage undoped AlGaN–GaN power HEMT on sapphire substrate and its demonstration for DC–DC converter application,"

IEEE Trans. Electron Devices **51** (11), 1913-1917 (2004).

[5] A. V. Vertiatchikh and L. F. Eastman, "Effect of the surface and barrier defects on the AlGaN/GaN HEMT low-frequency noise performance," *IEEE Electron Device Lett.* **24** (9), 535-537 (2003).

[6] D. Meng, S. Lin, C. P. Wen, M. Wang, J. Wang, Y. Hao, Y. Zhang, K. M. Lau and W. Wu, "Low leakage current and high-cutoff frequency AlGaN/GaN MOSHEMT using submicrometer-footprint thermal oxidized TiO_2/NiO as gate dielectric" *IEEE Electron Device Lett.* **34** (6), 738-740 (2013).

[7] L. Pang, Y. Lian, D.-S. Kim, J.-H. Lee and K. Kim, "AlGaN/GaN MOSHEMT with high-quality gate-SiO_2 achieved by room-temperature radio frequency magnetron sputtering," *IEEE Trans. Electron Devices* **59** (10), 2650-2655 (2012).

[8] O. Masaru, A. Mitsutoshi, O. Yutaka, K. Shigeru, M. Kouichi and M. Takashi, "AlGaN/GaN heterostructure metal-insulator-semiconductor high-electron-mobility transistors with Si_3N_4 gate insulator", *Jpn. J. Appl. Phys*. **42** (4B), 2278-2280 (2003).

[9] S. P. Singh, Y. Liu, Y. J. Ngoo, L. M. Kyaw, M. K. Bera, S. B. Dolmanan, S. Tripathy and E. F. Chor, "Influence of PECVD deposited SiN_x passivation layer thickness on $In_{0.18}Al_{0.82}N$/GaN/Si HEMT," *J. Phys. D: Appl. Phys.* **48** (36), 365104 (2015).

[10] M. A. Khan, X. Hu, A. Tarakji, G. Simin, J. Yang, R. Gaska and M. S. Shur, "AlGaN/GaN metal-oxide-semiconductor heterostructure field-effect transistors on SiC substrates", *Appl. Phys. Lett.* **77** (9), 1339-1341 (2000).

[11] Z. H. Liu, G. I. Ng, S. Arulkumaran, Y. K. T. Maung, K. L. Teo, S. C. Foo and V. Sahmuganathan, "Improved two-dimensional electron gas transport characteristics in AlGaN/GaN metal-insulator-semiconductor high electron mobility transistor with atomic layer-deposited Al_2O_3 as gate insulator", *Appl. Phys. Lett.* **95** (22), 223501 (2009).

[12] P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder and J. C. M. Hwang, "GaN metal-oxide-semiconductor high-electron-mobility- transistor with atomic layer deposited Al_2O_3 as gate dielectric," *Appl. Phys. Lett.* **86** (6), 063501 (2005).

[13] J. Shi and L. F. Eastman, "Correlation between AlGaN/GaN MISHFET performance and HfO_2 insulation layer quality", *IEEE Electron Device Lett.* **32** (3), 312-314 (2011).

[14] C. Liu, E. F. Chor and L. S. Tan, "Investigations of HfO_2/AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors," *Appl. Phys. Lett.* **88** (17), 173504 (2006).

[15] O. Seok, W. Ahn, M.-K. Han, and M.-W. Ha, "High on/off current ratio AlGaN/GaN MOS-HEMTs employing RF-sputtered HfO_2 gate insulators," *Semicond. Sci. Technol.* **28** (2), 025001 (2013).

[16] B. P. Downey, D. J. Meyer, D. S. Katzer, T. M. Marron, M. Pan and X. Gao, "Effect of SiN_x gate insulator thickness on electrical properties of $SiN_x/In_{0.17}Al_{0.83}N$/AlN/GaN MIS–HEMTs," *Solid-State Electron.* **106**, 12-17 (2015).

[17] B. S. Eller, J. Yang and R. J. Nemanich, "Electronic surface and dielectric interface states on GaN and AlGaN," *J. Vac. Sci. Technol. A* **31** (5) (2013).

[18] Z. Tang, Q. Jiang, Y. Lu, S. Huang, S. Yang, X. Tang and K. J. Chen, "600-V normally off SiN_x/AlGaN/GaN MIS-HEMT with large gate swing and low current collapse," *IEEE Electron Device Lett.* **34** (11), 1373-1375 (2013).

[19] T.-E. Hsieh, E. Y. Chang, Y.-Z. Song, Y.-C. Lin, H.-C. Wang, S.-C. Liu, S. Salahuddin, and C. C. Hu, "Gate recessed quasi-normally OFF Al_2O_3/AlGaN/GaN MIS-HEMT with low threshold voltage hysteresis using PEALD AlN interfacial passivation layer," *IEEE Electron Device Lett.* **35** (7), 732-734 (2014).

[20] J.-P. Ao, K. Nakatani, K. Ohmuro, M. Sugimoto, C.-Y. Hu, Y. Sogawa and Y. Ohno, "GaN metal–oxide–semiconductor field-effect transistor with tetraethylorthosilicate SiO_2 gate insulator on AlGaN/GaN

heterostructure," *Jpn. J. Appl. Phys*. **49** (4), 04DF09 (2010).

[21] Y. Wu, C. Y. Chen and J. A. del Alamo, "Electrical and structural degradation of GaN high electron mobility transistors under high-power and high-temperature Direct Current stress," *J. Appl. Phys.* **117** (2), 025707 (2015).

[22] K. Eriguchi and K. Ono, "Quantitative and comparative characterizations of plasma process-induced damage in advanced metal-oxide- semiconductor devices," *J. Phys. D: Appl. Phys.* **41** (2), 024002 (2008).

[23] D. G. Kent, K. P. Lee, A. P. Zhang, B. Luo, M. E. Overberg, C. R. Abernathy, F. Ren, K. D. Mackenzie, S. J. Pearton and Y. Nakagawa, "Electrical effects of N_2 plasma exposure on dry-etch damage in p- and n-GaN Schottky diodes", *Solid-State Electron.* **45** (10), 1837-1842 (2001).

[24] H. Wang, Y. Wang, G. Zhu, Q. Wang, Q. Xin, L. Han and A. Song, "A novel thermally evaporated etching mask for low-damage dry etching," *IEEE Trans. Nanotechnol.* **16** (2), 290-295 (2017).

[25] L. Yang, H. Wang, X. Zhang, Y. Li, X. Chen, X. Xu, X. Zhao and A. Song, "Thermally evaporated SiO serving as gate dielectric in graphene field-effect transistors", *IEEE Trans. Electron Devices* **64** (4), 1846-1850 (2017).

[26] F. Zhou, H. P. Lin, L. Zhang, J. Li, X. W. Zhang, D. B. Yu, X. Y. Jiang and Z. L. Zhang, "Top-gate amorphous IGZO thin-film transistors with a SiO buffer layer inserted between active channel layer and gate insulator," *Curr. Appl. Phys.* **12** (1), 228-232 (2012).

[27] G. Zhu, H. Wang, Y. Wang, X. Feng and A. Song, "Performance enhancement of AlGaN/AlN/GaN high electron mobility transistors by thermally evaporated SiO passivation," *Appl. Phys. Lett*. **109** (11), 113503 (2016).

[28] J. Wu, Y. Chen, D. Zhou, Z. Hu, H. Xie and C. Dong, "Sputtered oxides used for passivation layers of amorphous InGaZnO thin film transistors," *Mater. Sci. Semicond. Process*. **29**, 277-282 (2014).

[29] X. Xiao, W. Deng, X. He and S. Zhang, IEEE Trans. "a-IGZO TFTs with inductively coupled plasma chemical vapor deposited SiO_x gate dielectric," *IEEE Trans. Electron Devices* **60** (8), 2687-2690 (2013).

[30] C. M. Jeon and J.-L. Lee, "Effects of tensile stress induced by silicon nitride passivation on electrical characteristics of AlGaN/GaN heterostructure field-effect transistors," *Appl. Phys. Lett.* **86** (17), 172101 (2005).

[31] Y. Lv, Z. Lin, Y. Zhang, L. Meng, C. Luan, Z. Cao, H. Chen and Z. Wang, "Polarization Coulomb field scattering in AlGaN/AlN/GaN heterostructure field-effect transistors," *Appl. Phys. Lett*. **98** (12), 123512 (2011).

[32] J. Zhao, Z. Lin, T. D. Corrigan, Z. Wang, Z. You and Z. Wang, "Electron mobility related to scattering caused by the strain variation of AlGaN barrier layer in strained AlGaN/GaN heterostructures", *Appl. Phys. Lett.* 91 (17), 173507 (2007).

[33] S. Ganguly, J. Verma, G. Li, T. Zimmermann, H. Xing and D. Jena, "Presence and origin of interface charges at atomic-layer deposited Al_2O_3/III-nitride heterojunctions," *Appl. Phys. Lett.* 99 (19), 193504 (2011).

[34] D. Gregušová, J. Bernát, M. Držík, M. Marso, J. Novák, F. Uherek and P. Kordoš, "Influence of passivation induced stress on the performance of AlGaN/GaN HEMTs," *Phys. Stat. Sol. C* **2** (7), 2619-2622 (2005).

[35] T. B. Fehlberg, J. S. Milne, G. A. Umana-Membreno, S. Keller, U. K. Mishra, B. D. Nener and G. Parish, "Transport studies of AlGaN/GaN heterostructures of different Al mole fractions with variable SiN_x passivation stress," *IEEE Trans. Electron Devices* **58** (8), 2589-2596 (2011).

[36] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices* (John Wiley & Sons, Inc., Hoboken, New Jersey, 2006) P.315.

[37] H. Y. Shih, F. C. Chu, A. Das, C. Y. Lee, M. J. Chen and R. M. Lin, "Atomic layer deposition of gallium oxide films as gate dielectrics in AlGaN/GaN metal-oxide-semiconductor high-electron-mobility transistors",

Nanoscale Res. Lett. **11** (1), 235 (2016).

[38] R. Vetury, N. Q. Zhang, S. Keller and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *IEEE Trans. Electron Devices* **48** (3), 560-566 (2001).

[39] C. Liu, E. F. Chor, and L. S. Tan, "Enhanced device performance of AlGaN/GaN HEMTs using HfO_2 high-*k* dielectric for surface passivation and gate oxide," *Semicond. Sci. Technol.* **22** (5), 522-527 (2007).

[40] C. J. Kirkpatrick, B. Lee, R. Suri, X. Yang, and V. Misra, "Atomic layer deposition of SiO_2 for AlGaN/GaN MOS-HFETs," *IEEE Electron Device Lett.* **33** (9), 1240-1242 (2012).

[41] R. Wang, P. Saunier, Y. Tang, T. Fang, X. Gao, S. Guo, G. Snider, P. Fay, D. Jena and H. Xing, "Enhancement-mode InAlN/AlN/GaN HEMTs with 10^{-12} A/mm leakage current and 10^{12} on/off current ratio," *IEEE Electron Device Lett.* **32** (3), 309-311 (2011).

[42] P. Rottländer, M. Hehn and A. Schuhl, "Determining the interfacial barrier height and its relation to tunnel magnetoresistance", *Phys. Rev. B* **65** (5), 054422 (2002).

[43] L. Lugani, M. A. Py, J. F. Carlin and N. Grandjean, "Leakage mechanisms in InAlN based heterostructures," *J. Appl. Phys.* **115** (7), 074506 (2014).

[44] X. Y. Liu, S. X. Zhao, L. Q. Zhang, H. F. Huang, J. S. Shi, C. M. Zhang, H. L. Lu, P. F. Wang, and D. W. Zhang, "AlGaN/GaN MISHEMTs with AlN gate dielectric grown by thermal ALD technique," *Nanoscale Res. Lett.* **10**, 109 (2015).

[45] J. J. Freedsman, T. Kubo, and T. Egawa, "High drain current density E-mode Al_2O_3/AlGaN/GaN MOS-HEMT on Si with enhanced power device figure-of-merit," *IEEE Trans. Electron Devices* **60** (10), 3079-3083 (2013).

[46] T. Nakao, Y. Ohno, S. Kishimoto, K. Maezawa and T. Mizutani, "Study on off-state breakdown in AlGaN/GaN HEMTs," *Phys. Stat. Sol. C* **0** (7), 2335-2338 (2003).

[47] Y. Ohno, T. Nakao, S. Kishimoto, K. Maezawa and T. Mizutani, "Effects of surface passivation on breakdown of AlGaN/GaN high-electron- mobility transistors," *Appl. Phys. Lett.* **84** (12), 2184 (2004).

[48] C. K. Wang, R. W. Chuang, S. J. Chang, Y. K. Su, S. C. Wei, T. K. Lin, T. K. Ko, Y. Z. Chiou, and J. J. Tang, "High temperature and high frequency characteristics of AlGaN/GaN MOS-HFETs with photochemical vapor deposition SiO_2 layer," *Mat. Sci. Eng. B* **119** (1), 25-28 (2005).

[49] K.-W. Lee, K.-L. Lee, X.-Z. Lin, C.-H. Tu, and Y.-H. Wang, "Improvement of impact ionization effect and subthreshold current in InAlAs/InGaAs metal-oxide-semiconductor metamorphic HEMT with a liquid-phase oxidized InAlAs as gate insulator," *IEEE Trans. Electron Devices* **54** (3), 418-424 (2007).

[50] M. A. Alim, A. A. Rezazadeh, and C. Gaquiere, "Thermal characterization of DC and small-signal parameters of 150 nm and 250 nm gate-length AlGaN/GaN HEMTs grown on a SiC substrate," *Semicond. Sci. Technol.* **30** (12), 125005 (2015).

[51] G. Crupi, G. Avolio, A. Raffo, P. Barmuta, D. M. M. P. Schreurs, A. Caddemi, and G. Vannini, "Investigation on the thermal behavior of microwave GaN HEMTs," *Solid-State Electron*. **64** (1), 28-33 (2011).

[52] J.-S. Shi, H.-F. Huang, X.-Y. Liu, S.-X. Zhao, L.-Q. Zhang, and P.-F. Wang, "Effect of device geometry on static and dynamic performance of AlGaN/GaN-on-Si high electron mobility transistor," *Mater. Res. Express* **3** (8), 085013 (2016).