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PVT-Aware Sensing and Voltage Scaling for Energy Efficient FPGAs

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In this work we introduce a method to improve the energy efficiency of the FPGA devices by reducing the pessimistic operation guardbands posed by the commercial EDA tools. The proposed method bases on a voltage scaling scheme that reliably decreases the supply voltage. We deploy a uniform network of delay-based sensors across the fabric of the FPGA to sense all process, voltage and temperature variation (PVT) effects. The delay of all the sensors is calibrated to match the worst critical path delay of the target application. In that respect, the monitoring of the sensor network enables the indirect assessment of the functional integrity of the target application. The distributed placement of the sensors provides the desired sensitivity with appropriate granularity across the fabric and allows us to consider the worst-case scenario. The sensor network is integrated during the development cycle as a ready-to-use software IP with negligible resource overhead, for example, 1-2% of a Zynq XC7Z020 FPGA for 10 sensors. The sensitivity of the sensors to all PVT variations and the correlation with the application operation is verified through extensive testing by using multiple FPGAs and realistic benchmarks. The aforementioned approach facilitates a closed-loop voltage scaling scheme to regulate the supply voltage and reduce the power of the system. In our experiments on a set of 28nm Xilinx XC7Z020 SoC FPGAs and realistic digital signal processing (DSP) benchmarks, we demonstrate up to 27.2% decrease in power for 13% decrease in voltage, while retaining the nominal timing performance.

Keywords: FPGA; Voltage Scaling; Process Variation; Voltage Variation; Temperature Variation

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